intel®

APPLICATION NOTE

AP-12

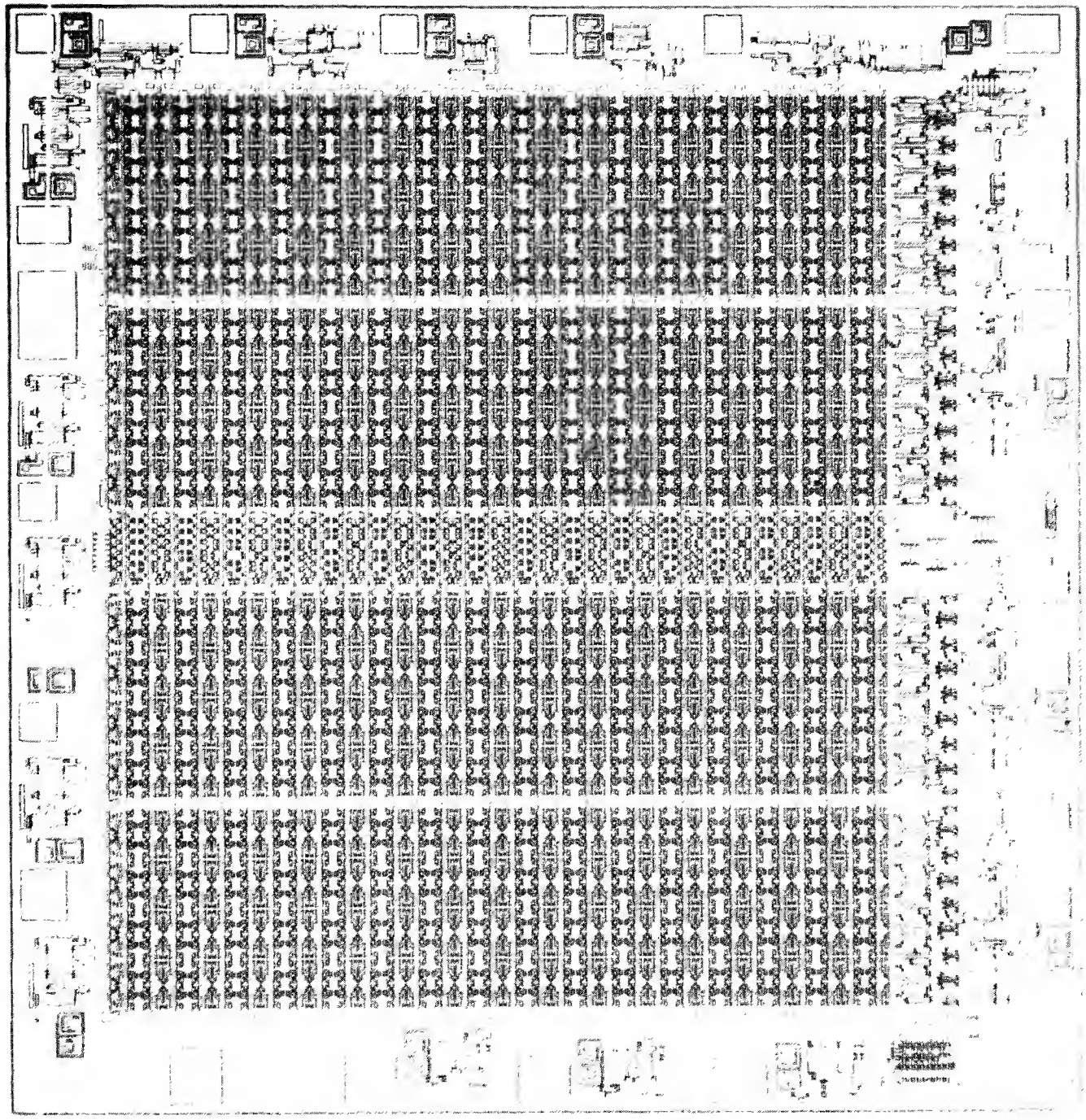
Designing Non-Volatile Memory Systems with Intel's 5101 RAM

Jim Oliphant
Application Engineering

Designing Non-Volatile Memory Systems with Intel's® 5101 RAM

Contents

Photomicrograph of 5101 CMOS RAM



INTRODUCTION

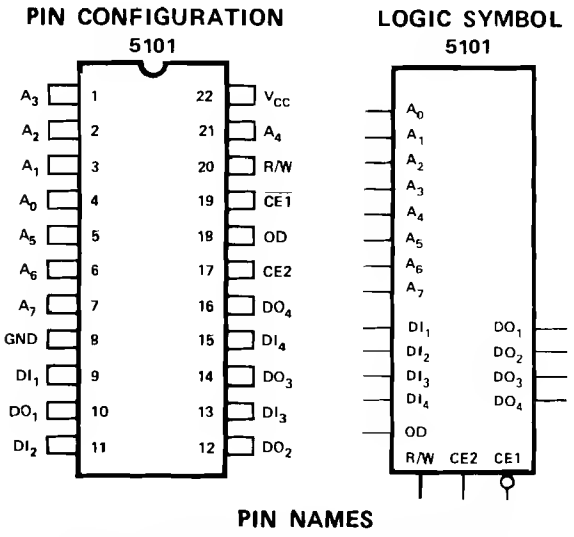
The Intel® 5101 is an ultra-low power 1024 bit static RAM organized as 256 words X 4 bits. It is fabricated with an advanced ion-implanted silicon gate CMOS technology. The 5101 is fully TTL compatible, uses only a single supply voltage V_{CC} (+5V) and does not require a clocking operation on the chip enable input. This device is ideally suited for low power and high speed applications where battery support for non-volatility is required.

The purpose of this application note is to describe the internal circuitry and operation of the 5101 and to outline various circuit techniques for battery supported non-volatile operation. In addition, designs using the 5101 will be described and the interface discussed.

DEVICE DESCRIPTION

The 5101 is pin compatible with the Intel® 2101 n-channel silicon gate static MOS RAM. The internal circuitry, however, differs from the 2101 in that the 5101 is implemented with CMOS technology and the 2101 is implemented with n-channel technology. (However, both the 5101 and 2101 are TTL compatible.) The pin configuration and logic symbol for the 5101 are shown in Figure 1. Memory expansion is simplified by the use of two chip enables $\overline{CE}_1$ and CE_2. CE_2 may be used to place the memory in the ultra low power standby mode completely independent of the state of *all* other inputs. In addition, an output disable pin is provided to place the internal data output buffers in a high impedance state. This is particularly useful in those systems which have a common data bus. Both the output disable and chip enable features will be discussed in more detail in the Systems Considerations section.

A block diagram for the 5101 is shown in Figure 2. The memory array is arranged in a 32 X 32 matrix. The five low order addresses A_0-A_4 select 1 of 32 rows; the three high order addresses A_5-A_7 select 1 of 8 column select lines. Each of the column select lines enable 4 of the 32 columns. Figure 3 shows a selection matrix for the selection of a given address to the 5101.



PIN NAMES

DI_1 - DI_4	DATA INPUT	OD	OUTPUT DISABLE
A_0 - A_7	ADDRESS INPUTS	DO_1 - DO_4	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)
$\overline{CE1}$, CE2	CHIP ENABLE		

Figure 1. 5101 Pin Configuration and Logic Symbol

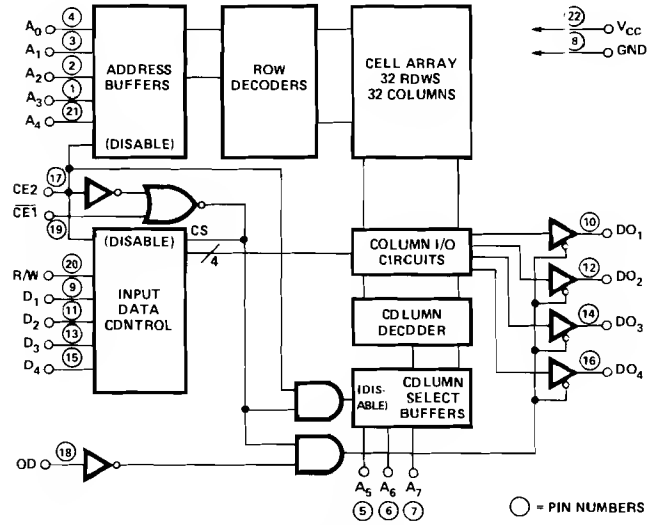


Figure 2. 5101 Block Diagram

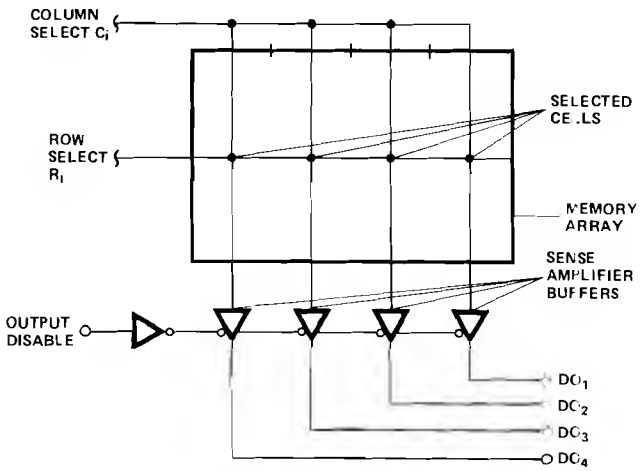


Figure 3. 5101 Selection Matrix

As shown in the block diagram, $\overline{CE_1}$ and CE_2 control the input data buffers and output data buffers. If either $\overline{CE_1}$ is high or CE_2 is low, the data-in and read/write buffers are disabled and the memory is isolated from the data in inputs. Likewise when either or both of the chip selects are in the non-select state (see Table I) the output buffers are placed in a high impedance state. When the chip is selected (i.e., $\overline{CE_1}$ is low and CE_2 is high), the output disable pin (OD) can be used to place the output buffers in a high impedance state.

Table I. 5101 Output State & Selection Matrix

OD	$\overline{CE_1}$	CE_2	Selection	Output
H	H	H	Deselected	High Imp.
H	H	L	Deselected	High Imp.
H	L	H	Selected	High Imp.
H	L	L	Deselected	High Imp.
L	H	H	Deselected	High Imp.
L	H	L	Deselected	High Imp.
L	L	H	Selected	Enabled
L	L	L	Deselected	High Imp.

Device Operation

STORAGE CELL

The storage cell used in the 5101 is implemented with 6 MOS transistors as shown in Figure 4. The six transistors are connected to form a cross-coupled latch which acts as the memory element. Note that the logic and gating transistors Q_1, Q_3, Q_5, and Q_6 are n-channel enhancement mode (normally off) MOS devices. The load transistors Q_2 and Q_4 are p-channel enhancement mode devices.

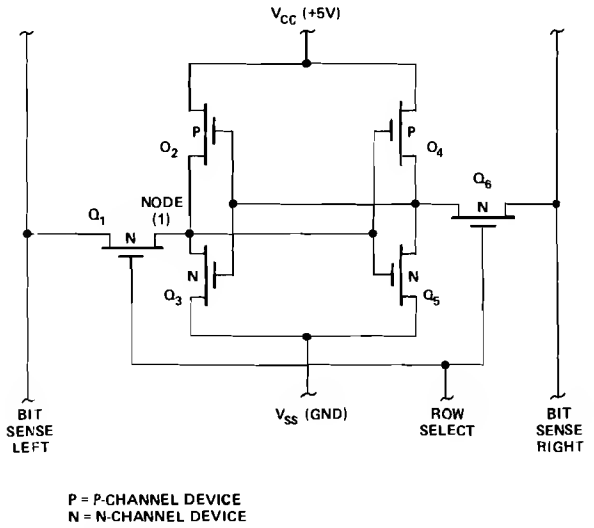


Figure 4. 5101 Storage Cell

In the following discussion of storage cell operation, remember that an n-channel device will be "on" if the gate is at a high level (~V_{CC}). A p-channel device will be "on" if its gate is at a low level (~GND). Operation of the storage cell is as follows:

Assume that the gate of Q_3 is at a high level (V_{CC}), device Q_3 is therefore turned on (it is an n-channel device) while device Q_2 is turned off (it is a p-channel device). Node (1) is therefore pulled to V_{SS} (ground) and cross-coupled back to the gates of devices Q_4 and Q_5. This low level on node (1) will turn device Q_4 on and Q_5 off. Since the output of Q_4-Q_5 is fed back to the gates of Q_2 and Q_3, an initial charge of V_{CC} on the gate of Q_3 will hold the latch in the above state. This logic state (node 1 at GND) is defined as a "1". The cell contains a logic "0" if the gate of Q_4 and Q_5 is high (V_{CC}) which puts node (1) at V_{CC}. Table II summarizes the state of the memory cell for a logic "1" and logic "0".

Table II. 5101 Memory Cell State

Cell State	Q_2	Q_3	Q_4	Q_5
Logic "0"	On	Off	Off	On
Logic "1"	Off	On	On	Off

Note that in the above discussion no mention was made of any d.c. currents flowing to set the proper voltage levels in the latch. This is because there aren't any. For the example given, the gate of Q_3 is held high (V_{CC}) by device Q_4 (the p-channel load). Since Q_5 is off there is no d.c. path for the current to take in the quiescent state. The only current flowing is the junction leakage currents associated with the source/drain of the MOS devices. This current is typically in the nano-ampere range.

The memory cell is accessed for a read or write operation by activating the appropriate row select line (i.e. row select is brought to V_{CC}). This turns on devices Q_1 and Q_6 and allows data on the bit sense lines to be written into the cell or the state of the cell to be interrogated (read) by a sense amplifier placed on the bit sense lines. For a write operation Bit Sense right is set high (V_{CC}) to write a "1" or Bit Sense left is set high (V_{CC}) to write a "0". The opposite Bit Sense line is held low (V_{SS}).

ADDRESS BUFFER

The address buffers translate the low level TTL address inputs (V_{IL} max. = 0.65V, V_{IH} min. = 2.2V) to a CMOS level (high = V_{CC}, low = V_{SS}) for internal use. The buffer configuration used is shown in Figure 5.

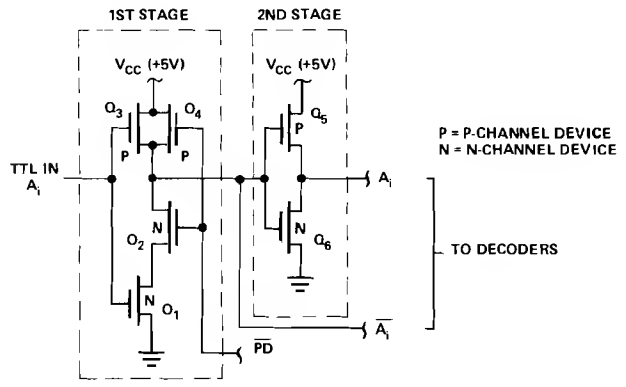


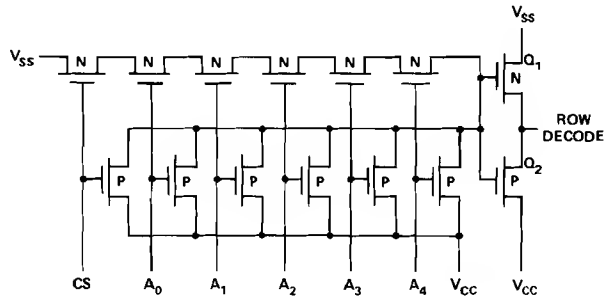
Figure 5. 5101 TTL Address Buffer

The first stage of the address buffer consists of a NAND gate (Q_1, Q_3) with control gates (Q_2, Q_4) added to *disconnect* the TTL address from the decoders when the device is not selected (that is, CE_2 is low). This places the address buffers in a standby mode (only leakage currents flowing) and eliminates the need to control the state of the addresses during standby. The internally generated signal $\overline{PD}$ which blocks the input addresses from the internal decoders is generated from CE_2. The second stage is an inverting buffer to provide increased drive for the A_i addresses.

Note that when the device is in a quiescent state no d.c. current is being drawn by the buffer. Therefore, the power dissipated during operation is very small and amounts to only the leakage current associated with the source/drain p-n junctions.

DECODERS

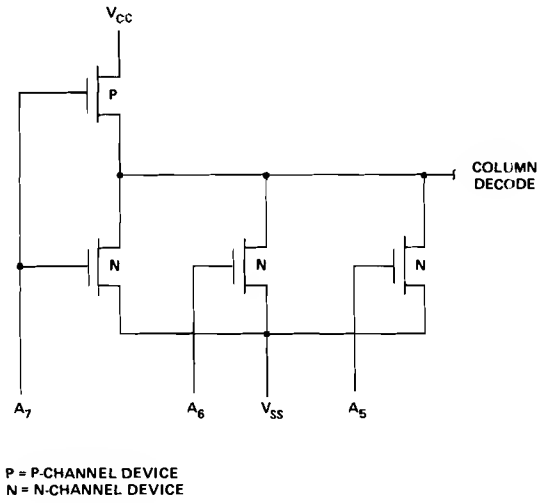
The row decoders (selecting 1 of 32 rows) on the 5101 use an AND gate of the type shown in Figure 6. To activate the selected row decode line, the five addresses going to that particular decoder must be at a high level and the internal chip select (CS) must be high. (Chip select is formed by the logical AND of CE_2 and $\overline{CE_1}$). If all address inputs to the decoder are high, a low is placed on the gates of the inverter buffer (devices Q_1 and Q_2) which will turn Q_1 off and Q_2 on. The selected row decode line is thereby brought high, turning on the appropriate gates in the selected memory cells. If the device is not selected, then CS forces all row decoder lines low which disables any access to all memory cells.



P = P-CHANNEL DEVICE
N = N-CHANNEL DEVICE
CS = $\overline{CE1} \cdot CE2$

Figure 6. 5101 Row Decode

The column decoders use a NOR type gate shown in Figure 7. The selected column decode line goes high if the 3 addresses (A_5-A_7) being decoded are all at a low level. Note that the internal column decoder uses only three address inputs. These three inputs select 1 of 8 separate decode lines. Each of the 8 decode lines select 4 columns for each word addressed.



P = P-CHANNEL DEVICE
N = N-CHANNEL DEVICE

Figure 7. 5101 Column Decode

INTERNAL DATA SENSING

A simplified schematic of the 5101 column sense amplifier is shown in Figure 8. The sense amplifier is constructed in an AND configuration with the I/O left line of each column of memory cells AND'ed with a particular column decode (devices Q_1 and Q_2). The line to the output buffer, O_B, is held at V_{CC} by device Q_3 unless both the I/O left line *and* the column decode line (for that particular column) are both high (logic "0" in the memory cell). In this case, the output of the sense amplifier O_B will be driven to a low level (slightly above GND). For example, if memory cell "M" shown in Figure 8 contained a "0" (I/O left high) then O_B would be low. However, if "M" contained a "1" (I/O left low) then O_B would remain high.

Devices Q_4 and Q_6 shown in Figure 8 are used as a load on the particular I/O line. The n-channel devices (Q_5 and Q_7) are used to limit the logic swing on the I/O lines.

Data is written into the memory cell by the circuitry shown in Figure 8. Note that the I/O right line goes high only when a logic "1" (high level) is applied to the data-in input on a selected device during a write cycle. The I/O left line, however, goes high when either a low is on the data-in input or the chip is non-selected. (Recall that for a non-selected device, all row selects are at the non-selected state, i.e. low level.)

OUTPUT BUFFER

A simplified schematic for the 5101 output buffer is shown in Figure 9. As shown in this figure the output buffer is implemented with complementary n-channel and p-channel drivers. For this type of driver, the gates of devices Q_1 and Q_2 must be at the same logic level (high or low) so that one of these devices is on while the other is off for a nor-

mal read operation. However, when the chip is deselected (the internal CS is low) or output disable is high, both Q_1 and Q_2 are turned off and the Data Out output goes to a high impedance state.

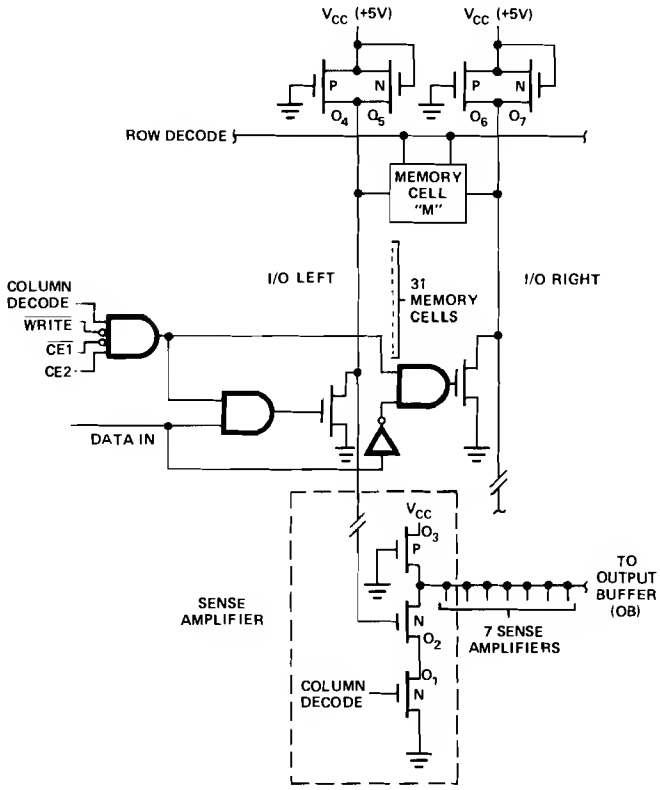


Figure 8. 5101 Column Sense Amplifier

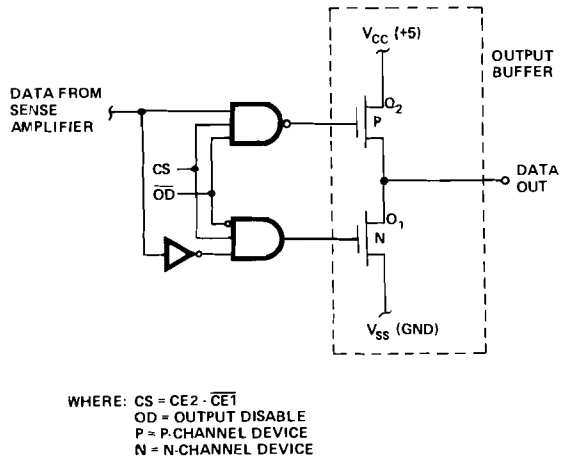


Figure 9. 5101 Output Buffer

Device Specifications

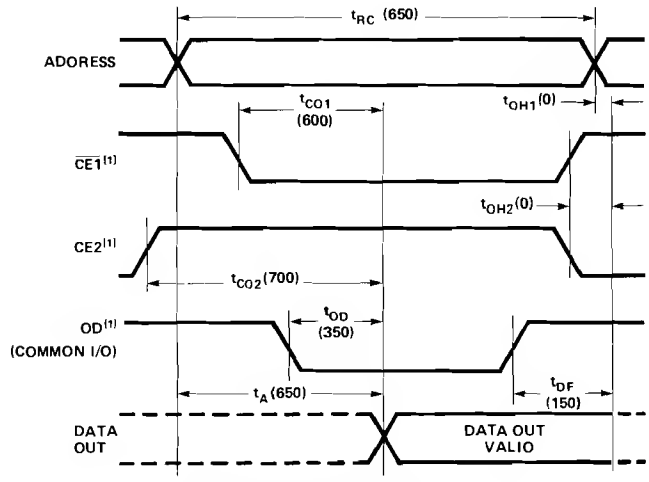
READ CYCLE

Minimum timing for a 5101 read cycle is shown in Figure 10. This timing diagram shows the relationship of all necessary control signals required for a read cycle and is for a general application. However, if the user has certain flexibilities in his system, other modes of operation are possible.

For those systems which have separate data inputs and outputs in the memory array, the output disable input (pin 18) may be tied low. Also, if the input and output pins of the 5101 are not OR tied to any other device both chip enable inputs may be held true (i.e. $\overline{CE_1}$ is held low and CE_2 is held high) while the addresses are being cycled in any order for a series of read cycles. For this case, the read/write input must be held high throughout the read operations. However, when operating the 5101 with CE_2 held high, it is necessary to control the voltage level of all inputs if ultra low power dissipation is desired. The ultra low standby power can be achieved with $\overline{CE_1}$ *only* deselected (i.e. at a high level) by holding all address, chip enable, data-in and read/write inputs to *one* of the following levels:

1. $V_{in} \leq 0.2V$
2. $V_{in} \geq V_{CC} - 0.2V$

Note that $\overline{CE_1}$ may be tied low, if so desired, and the ultra low standby power controlled only with CE_2 (i.e. $CE_2 \leq 0.2V$, all other inputs in a "don't care" state). The definition of terms outlined in Figure 10 is contained in Table III.



1. SEE TEXT "READ CYCLE".
2. NUMBERS IN PARENTHESES ARE IN NSEC.

Figure 10. 5101 Read Cycle

Table III. 5101 Read Cycle A.C. Characteristics. $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	650			ns	Input Pulse Levels +0.65V to 2.2V. Input Pulse Rise and Fall Times 20 nsec. Timing Measurement Reference Level 1.5V. Output Load 1 TTL Gate and $C_L = 100pF$.
t_A	Access Time			650	ns	
t_{CO1}	Chip Enable ($\overline{CE1}$) to Output			600	ns	
t_{CO2}	Chip Enable (CE2) to Output			700	ns	
t_{OD}	Output Disable To Output			350	ns	
t_{DF}	Data Output to High Z State	0		150	ns	
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0			ns	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns	

Table IV. 5101 Write Cycle A.C. Characteristics. $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	650			ns	Input Pulse Levels +0.65V to 2.2V. Input Pulse Rise and Fall Times 20nsec. Timing Measurement Reference Level 1.5V. Output Load 1 TTL Gate and $C_L = 100pF$.
t_{AW}	Write Delay	150			ns	
t_{CW1}	Chip Enable ($\overline{CE1}$) To Write	550			ns	
t_{CW2}	Chip Enable (CE2) To Write	550			ns	
t_{DW}	Data Setup	400			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

WRITE CYCLE

Minimum timing for a 5101 write cycle is shown in Figure 11. The waveforms shown in Figure 11 are for a general application of the 5101 during a write cycle and may be modified to some degree depending on the users requirements. For example, if no other data inputs or outputs are OR tied to the 5101, $\overline{CE_1}$ may be held low, CE_2 held high and output disable held low.

However, it is *not* permissible to hold the read/write line low while cycling through addresses for a series of write cycles. Attempting to perform a series of write cycles in this manner will result in writing into multiple address locations during address transitions.

Although it is not necessary to conform exactly to the waveforms shown in Figure 11 for a write cycle, care should be taken to assure all minimum timing constraints, listed in Table IV, are adhered to. Particular attention should be paid to T_{aw} (address to write set-up time), T_{cw1} and T_{cw2}.

Since the 5101 is a completely static random access memory, it does not require an edge on any input line (e.g. chip enable or address) to initiate a cycle. Therefore, when a device is enabled (i.e. $\overline{CE_1}$ is low and CE_2 is high) and addresses are changed, time must be provided for the row and column decoders to settle (T_{aw}) before commencing a write to make sure undesired address locations are not partially rewritten by the data on the data input line.

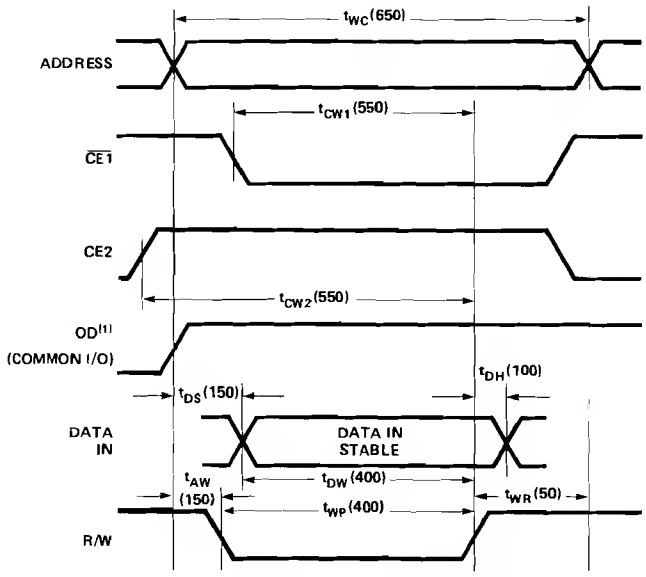


Figure 11. 5101 Write Cycle

Table V. D.C. Operating Characteristics. T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current		5		nA	V_{IN} = 0 to 5.25V
I_{LOH}	Output High Leakage			1	μA	$\overline{CE1}$ = 2.2V, V_{OUT} = V_{CC}
I_{LOL}	Output Low Leakage			1	μA	$\overline{CE1}$ = 2.2V, V_{OUT} = 0.0V
I_{CC1}	Operating Current		9	22	mA	V_{IN} = V_{CC} Except $\overline{CE1} \leq$ 0.01V Outputs Open
I_{CC2}	Operating Current		13	27	mA	V_{IN} = 2.2V Except $\overline{CE1} \leq$ 0.65V Outputs Open
I_{CCL}[2]	Standby Current			15	μA	V_{IN} = 0 to V_{CC}, Except CE2 ≤ 0.2V
V_{IL}	Input "Low" Voltage	-0.3		0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = 1.0mA

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage.
2. Current through all inputs and outputs included in I_{CCL}.

Table VI. 5101L Low V_{CC} Data Retention Characteristics. T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V	CE2 ≤ 0.2V	
I_{CCDR}	Data Retention Current			15	μA		V_{DR} = 2.0V
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[2]			ns		

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage.
2. t_{RC} = Read Cycle Time.

D.C. OPERATING CHARACTERISTICS

The D.C. operating characteristics of the 5101 are given in Table V. I_{CCL} (standby current) in Table V is emphasized because of its importance in standby battery back-up operation. Note that the maximum value of the standby power supply current is an extremely low 15μA (and is typically only 0.2μA). If CE_2 is used to control the low power state (i.e. $CE_2 \leq$ 0.2V), then the state of all other inputs is a "don't care." If $\overline{CE_1}$ is used to control the low power state, all inputs must be either high or low (as defined in Read Cycle section). As is shown later, (in the Systems Considerations section) this allows the designer maximum flexibility in the design of simple battery interfaces to implement a battery back-up system.

As shown in Table V, the 5101 is capable of driving a maximum TTL load of 2mA at an output voltage V_{OL} of 0.4V. Attempting to sink more than 2mA will result in an increased V_{OL}.

LOW V_{CC} DATA RETENTION

The 5101L family of RAMs has ultra low standby current and requires only that V_{CC} be between 2.0V ≤ V_{CC} ≤ 5.25V to maintain data. As shown, these devices are guaranteed to operate in a standby mode with V_{CC} a minimum of 2.0V. Table VI gives the low V_{CC} data retention characteristics of the 5101L. The waveforms for low V_{CC} data retention operation are shown in Figure 12.

As shown in Figure 12, CE_2 must be brought low (≤0.2V) at or before the V_{CC} supply drops to 4.75V. In addition, CE_2 must remain in the low

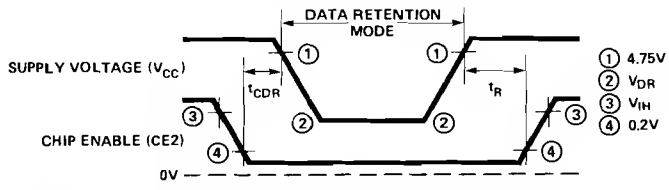


Figure 12. Low V_{CC} Data Retention Waveforms

state for a period equal to a read cycle time after V_{CC} has reached a minimum of 4.75V after power-up. It is important to note that the supply voltage V_{CC} does *not* have to be reduced below 4.75V as shown in Figure 12. Remember that the standby current I_{CCL} is a maximum of 15μA up to V_{CC} = 5.25V. The typical data retention current as a function of V_{DR} (V_{CC} in data retention mode) is shown in Figure 13.

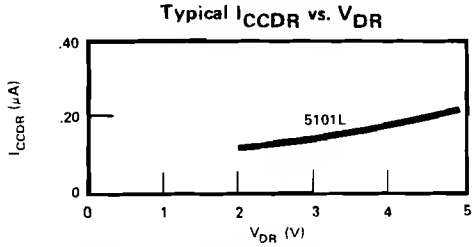


Figure 13. 5101L Data Retention Current Vs. V_{DR}

SYSTEMS CONSIDERATIONS

Since the 5101 is a completely static TTL compatible random access memory device requiring no clocks, refresh or special drivers/sense circuitry, the designer can treat the 5101 as any other TTL compatible device. Because of the ease with which the 5101 can be used, this section on Systems Considerations will concentrate on circuitry associated with battery-supported standby operation. Discussions of any interface buffers (if required) to a 5101 system will be relative to the effect these buffers have on the standby power source (e.g. battery) and what can be done to minimize the adverse effects of the buffers. Additional information regarding buffers for static TTL compatible RAMs can be found in Intel's Application Note AP-8, "Designing with Intel's Static MOS RAMS".

Low Power Standby Operation

When designing a non-volatile semiconductor memory system, the basic requirements can be outlined as follows:

1. Maximum data retention time-battery back-up.
2. Maximum load current during standby-data retention mode.
3. Physical size requirement of battery.
4. Access/cycle time (operating mode).

Access time is important as it effects the selection of address and data buffers required by the system. If high speed operation is desired, it may be necessary to use series 74S type gates for the buffers. If speed is not of primary interest then CMOS type buffers may be used. Clearly, TTL type buffers will draw considerably more power than CMOS buffers if left connected to the battery supply during the data retention mode. The battery interface to both TTL and CMOS buffers will be discussed in the battery section.

The required data retention time for battery supported standby operation is of primary importance in the selection of a battery. The usual trade-offs associated with data retention time are:

1. Memory size (number of words that must be non-volatile).
2. Physical battery size desired (determines if the battery is to be placed on a printed circuit card or is external to the card).

Within reasonable constraints of memory size and data retention time, there are many types and configurations of batteries that can be used.

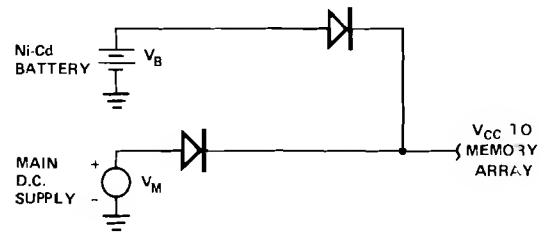
Power Switching

Two basic types of power switching circuits (switching between the main supply and the battery) are described which are simple and inexpensive.

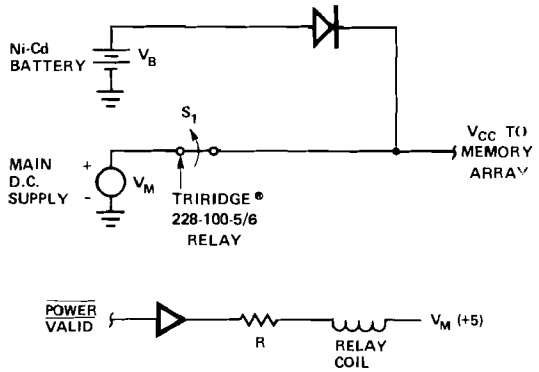
These two types are:

1. Diode Coupled
2. Switch Coupled

These two types of switching circuits are shown in Figure 14. The diode coupled circuit requires the main d.c. supply to be above the required V_{CC} voltage by the amount of drop through the diode. The diode used should have a low forward drop (such as found in Germanium diodes) and low series resistance.



A. Diode Coupled



B. Switch Coupled

Figure 14. Power Switching Circuits

If it is not desirable to have a power supply voltage above V_{CC} (e.g. existing +5.0V supplies are to be used), then a normally open switch can be used in place of the diode. The switch is held closed by a simple TTL buffer gate as shown in Figure 14 as long as $\overline{\text{POWER VALID}}$ is held low. When power loss is detected (see Power Loss Detect Section) the switch is opened and the battery automatically supplies power to the memory array. (Note that if the memory is to be used for a short period to load memory, etc., after $\overline{\text{POWER VALID}}$ goes high a delay must be included in the switch line to take power from the supply before it drops below 4.75V).

Power Loss Detect

In memory systems which have TTL interface and other control circuitry, it is usually necessary to have advanced warning that A.C. power has been lost. This allows the orderly shut down on the system and can provide time to store data/records in the non-volatile portion of memory. Such a circuit is shown in Figure 15.

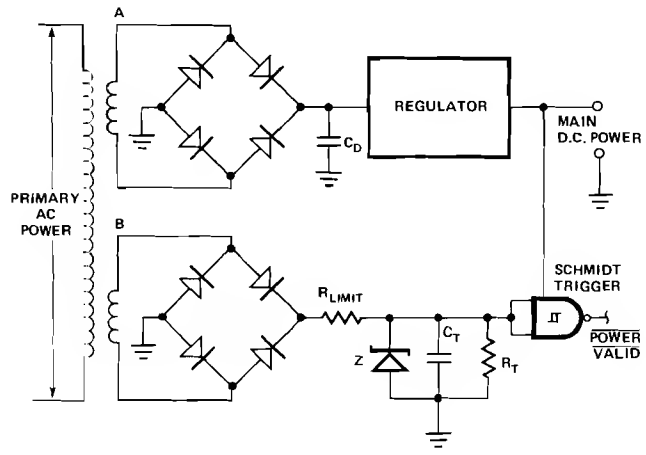


Figure 15. Power Loss Detect Circuit

The detect circuit uses a separate transformer winding (available on many power supplies) to provide a positive (≈+5V) voltage reference to a schmidt trigger. A separate winding is used so as not to interfere with the regulation of the main d.c. power source.

Operation of the detect circuit is as follows:
A high level (≈ 5V) is established at the input of a schmidt trigger (e.g. 7414) by the diode bridge network and zener Z. Resistor R_{LIMIT} is a current limiting resistor between the bridge and schmidt trigger input network. The R_T C_T combination controls the discharge rate of the input voltage to the schmidt trigger when reference power is lost. The time constant is used to prevent short (a few cycles) a.c. power loss from shutting down the system. The only restriction on the maximum value of the time constant is the $\overline{\text{POWER VALID}}$ signal must go high before the main d.c. power source drops below the minimum allowable operating voltage of the main d.c. source.

In general it is not desirable to combine the power loss detect circuitry with the main d.c. power source for two reasons:

1. Adverse effect on d.c. output regulation by R_{LIMIT} resistor, and
2. The large decoupling capacitor, C_D, on most d.c. supplies.

The large decoupling capacitor C_D will cause a time constant which is too large and may not allow sufficient time between $\overline{\text{POWER VALID}}$ going high and the main d.c. power dropping below acceptable minimums

Batteries For Non-Volatile Semiconductor Memories

The first place to begin in the selection of a battery for a particular application is to analyze those factors dictated by system requirements and fit the battery to the requirement. Some of these important criteria are:

1. Load current imposed on battery.
2. Battery voltage-full charge.
3. Battery voltage-end of life.
4. Life of battery under maximum load conditions.
5. Environment-temperature range (operating, non-operating).
6. Physical factors (size, weight).
7. Battery operation.

Of the seven criteria listed above, the one most likely to be overlooked is the effect of temperature on the capacity and life of the battery. For many batteries commerical grade temperature requirements (0° C to 70° C) may adversely effect both the capability and life of the battery.

Criteria seven, battery operation, refers to the operating schedule the battery is expected to meet. For example, if the battery is expected to maintain data *only* on a.c. power outages which are assumed to be rare, then a rechargeable battery (secondary cell) with a slow recharge rate may be selected. For this case, it may even be desirable to use a non-rechargeable battery (primary cell) with battery replacement scheduled at appropriate intervals (six months to 1 year).

However, if the system is operated in a mode where power is turned on in the morning and off in the evening then fast rechargeable batteries (with appropriate recharging circuity) may be required.

In the evaluation of the seven criteria listed previously, one of the first things to be determined is what type of battery is to be used in the system. The chart shown in Table VII outlines the characteristics of various storage cell types. Consider first the primary type.

PRIMARY BATTERIES (NON-RECHARGEABLE)

The use of primary batteries in a memory system is usually limited to those systems which require standby data retention infrequently or where very high battery capacities (mA-hr) and very small battery physical size are required. For these cases, both mercury and silver-oxide batteries offer large capacity combined with very small phsyical size. The small size of these batteries is shown in Figure 16 for a silver-oxide battery (110mA-hr).

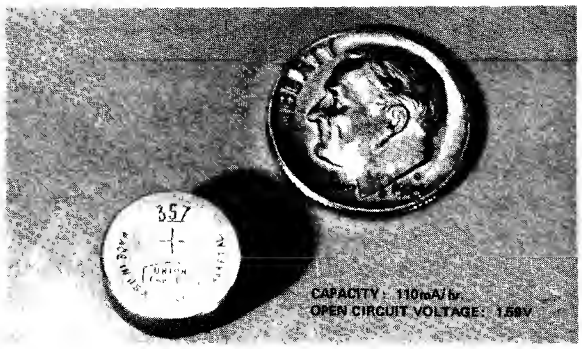


Figure 16. Silver-Oxide Button Cell

Typical voltage discharge curves for silver-oxide and mercury batteries are shown in Figures 17 and 18 respectively. Note that in both cells, the cell voltage remains nearly constant during discharge — a highly desirable characteristic. In addition, the mercury cell generally has greater capacity for a given size as compared with a silver-oxide battery.

Carbon-zinc batteries offer the lowest cost of any primary battery described, but suffer from a severe degradation of output voltage as a function of use. This characteristic makes carbon-zinc batteries undesirable for most standby power applications.

Alkaline batteries have a much better discharge characteristic than carbon-zinc, but are not quite as

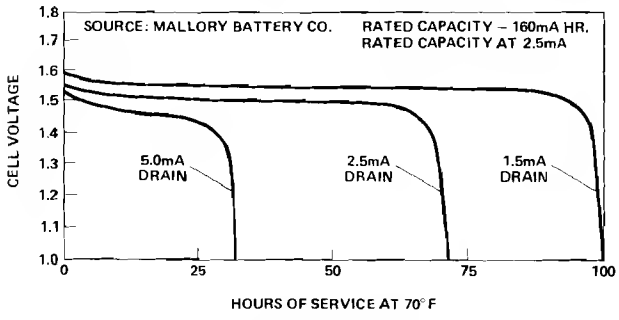


Figure 17. Silver-Oxide Cell Typical Voltage Discharge Characteristics

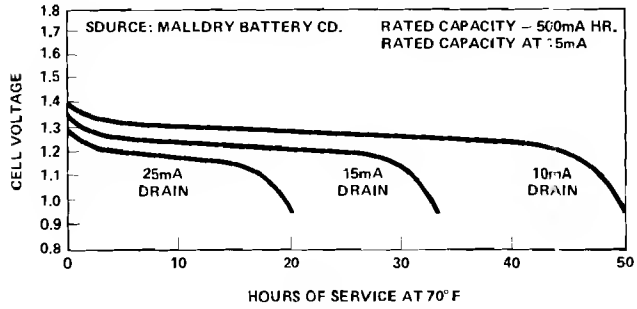


Figure 18. Mercury Cell Typical Voltage Discharge Characteristics

good as mercury or silver-oxide. The relative low cost of these batteries can make them attractive for use in some systems applications.

Both carbon-zinc and alkaline batteries are discussed in detail in the Eveready Battery Applications Engineering Data handbook (see Bibliography 3). It is emphasized that adequate attention should be directed to the output voltage characteristics of these two batteries before using them in a standby power application.

Because of printed circuit board area limitations small battery size is usually the reason for selecting a primary cell for battery support. In this case, it may be desirable to limit the number of cells in a particular system to one. However, this requires that a voltage boost circuit be used in the system to achieve a minimum sustaining voltage of 2.0V at end of battery life to operate the 5101. Such a boost circuit is shown in Figure 19.

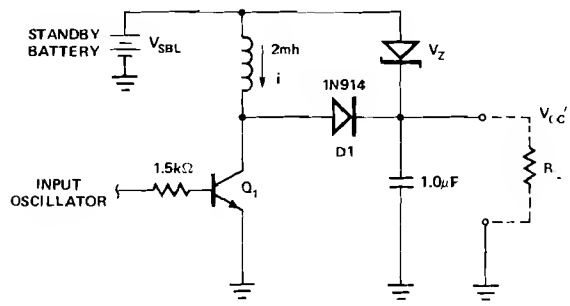


Figure 19. Basic Voltage Boost Circuit

Voltage Boost

Operation of the voltage boost circuit is as follows:

The input to Q_1 is a low duty-cycle signal. This signal turns Q_1 on forcing current through inductor L. When Q_1 is turned off, current i cannot change instantaneously and is diverted through diode D,

Table VII. Battery Characteristics

I. PRIMARY TYPE (NON-RECHARGEABLE)[1]

Cell Construction	Cell Voltage (Typ.)[2]	Comments
Carbon-Zinc (Leclanche)	1.5	Lowest cost; discharge characteristics may be inadequate for some systems
Silver-Oxide	~ 1.6	Good for low temperature operation, discharge characteristic excellent for most system requirements
Mercury	1.4	Good for high temperature operation, discharge characteristic excellent for most systems, long shelf life
Alkaline	1.5	Good efficiency for use with systems requiring total battery operation

II. SECONDARY TYPE (RECHARGEABLE)

Cell Construction	Cell Voltage (Typ.)	Comments
Nickel-Cadmium	1.2	Excellent all around characteristics for battery back-up, widely used
Lead-Calcium	2.0	Excellent all around characteristics for battery back-up

[1] Some information in this table condensed from "EVEREADY" Battery Applications and Engineering Data Handbook copyrighted 1971 by Union Carbide Corporation.

[2] Cells can be put in series to obtain multiples of basic cell voltage.

charging capacitor C. The voltage to which C charges is a function of the capacitance C, load R_L and zener V_Z.

In order to minimize the load on the battery and to maximize the efficiency of the boost circuit, it is necessary to turn on Q_1 only for the minimum amount of time which will still maintain the desired output standby voltage. Such a circuit is useful only if there is a way to power the input oscillator required for Q_1 off the same battery V_{SB}. Such a circuit is shown in Figure 20. The 5801, shown in Figure 20, is a low voltage CMOS oscillator made by Intel (used extensively by Microma, an Intel subsidiary). The output of this oscillator triggers a CMOS single-shot which in turn drives the voltage boost circuit shown in Figure 19. Note that the 5801 is powered by the battery (Cell voltage = 1.5V) and the 4047 (CMOS single-shot) is powered by the boosted V_{CC}'. It is, therefore, necessary to

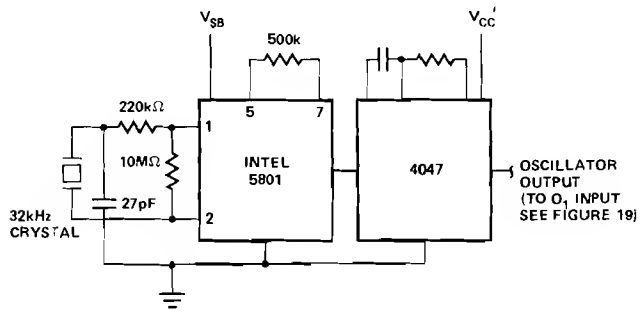


Figure 20. Voltage Boost Oscillator Circuit

assure that the standby voltage V_{CC} does not fall below 3V (minimum 4047 operating voltage) before starting the oscillator circuit. A power loss detect circuit can be used to warn of an impending power down condition and allow the boost circuit to be turned on in time to hold the V_{CC} voltage to $\cong$3V.

As stated previously, the power conversion efficiency of the oscillator and voltage boost circuits should be maximized to minimize the current drain on the battery. The efficiency of these circuits is largely a function of the duty cycle of the oscillator. Figure 21 shows the waveforms of the input signal to the voltage boost circuit and the current i through inductor L. A summary of the data in Figure 21 is shown in the graphs of Figure 22. Note that the curve of V_{CC}' levels out at 4.0V, this is the result of the clamp zener V_Z (Figure 19). Also note that the efficiency is markedly decreased as the input pulse to Q_1 is lengthened. For a given duty cycle on Q_1, the efficiency of the voltage boost circuit will increase if the load current is reduced.

SECONDARY BATTERIES (RECHARGEABLE)

As outlined in Table VII there are two basic types of rechargeable batteries ideally suited for memory system standby power-down operation. Nickel-Cadmium (Ni-Cd) and Lead-Calcium (such as Gel/Cell®). This section will outline some of the salient features of each type. No attempt will be made to compare the two for general operation. It is recommended that the system designer interface directly with the battery manufacturer to obtain guaranteed specification data, operating limitations and safety precautions (if any).

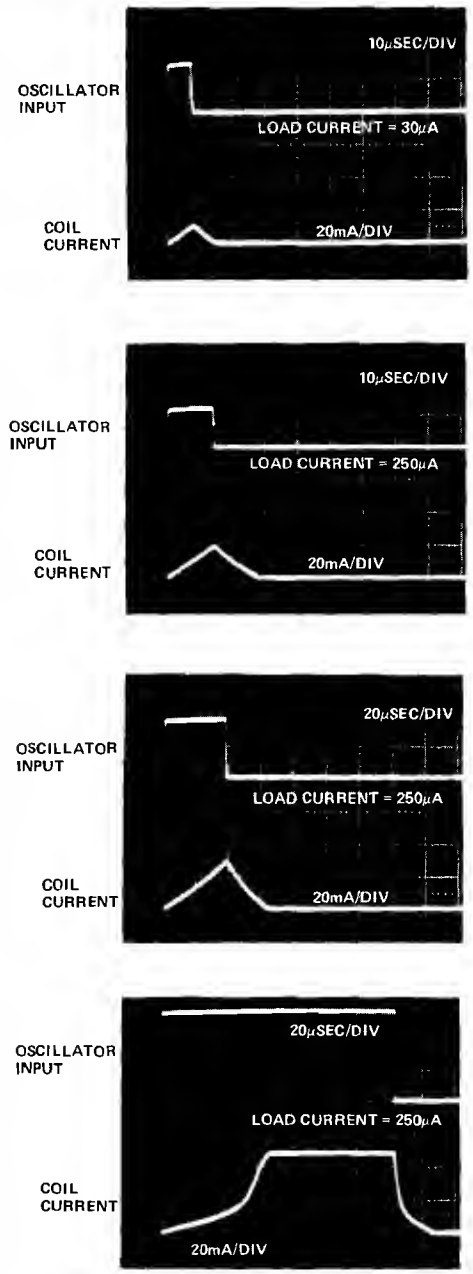


Figure 21. Voltage Boost Waveforms

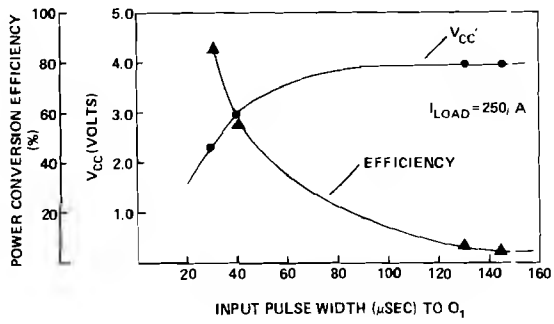


Figure 22. Boost Circuit Output Voltage and Efficiency Vs. Input Pulse Width

Photograph courtesy of General Electric Co.

Figure 23. Sizes of Selected Cylindrical Ni-Cd Batteries

Nickel-Cadmium

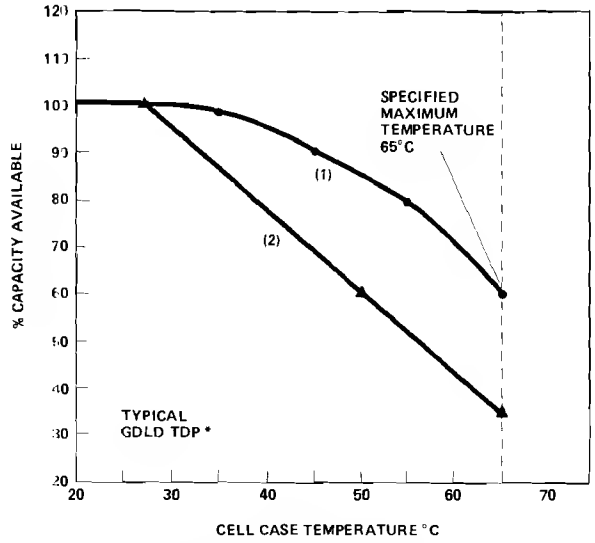
Nickel-Cadmium batteries are available in a wide variety of capacities (mA-hr) sizes and styles (see Figure 23). The styles include button, cylindrical and rectangular cells and may be placed on the memory printed circuit card or in the same enclosure as the main d.c. power supply. (Enclosing the batteries in with the main d.c. supply is usually done only in large back-up capacity systems.)

There are many manufacturers of Ni-Cd batteries who can supply the desired battery configuration. A useful place to begin looking for a battery supplier is Electronic Buyers Guide (McGraw-Hill publications.) (Also see bibliography.)

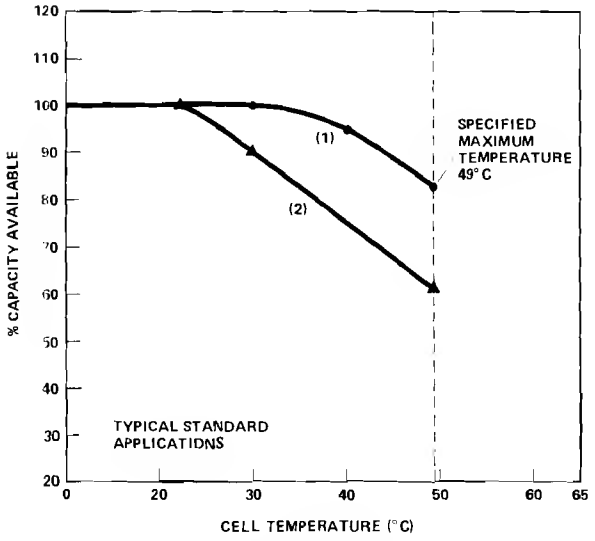
Electrical Characteristics

Electrical characteristics such as capacity (mA-hr) and cell voltage as a function of discharge rate for Ni–Cd batteries are temperature dependent. It is important for the designer to realize that high system operating temperatures may have an adverse effect on battery life and capacitance even though the battery is not expected to be called on to provide standby power at those temperatures.

An example of the effect of temperature on capacity (based on GE battery specifications) is shown in Figure 24 for two types of General Electric Ni-Cd batteries. Note that two types of usage are given: one for infrequent discharge with extended periods



* GOLD TDP IS A REGISTERED TRADEMARK OF GENERAL ELECTRIC.



NOTES:
(1) INFREQUENT DISCHARGE, EXTENDED PERIOD OF OVERCHARGE.
(2) FREQUENT DISCHARGE.

Figure 24. Ni-Cd Battery Capacity as a Function of Temperature

of overcharging, condition (1), the other for frequent discharge, condition (2). In most memory applications condition (1) will apply, which is the condition for maximum capacity as a function of temperature.

Ni-Cd batteries also have a self discharge characteristic which is a function of temperature. One result of this characteristic is that these types of batteries should not be stored in a charged condition for an appreciable length of time. Therefore, before inserting these batteries into a system or after the system has been powered down for an extended time (i.e. no trickle charge available and batteries disconnected from load) care must be exercised to assure that the batteries have sufficient charge to perform in a power down standby mode. In addition, when calculating the capacity of the battery for a particular load, the self discharge characteristic of the battery must be included. This self discharge rate can be as high as approximately 7%/day loss of capacity at 50°C to an average of 1%/day at room temperature (25°C) for Ni-Cd batteries.

The discharge characteristics of Ni-Cd batteries are flat, making them ideal for use in memory systems requiring standby power. The general shape of such characteristics is shown in Figure 25. Note that no scales are given in this figure because the output voltage as a function of time varies between manufacturers of Ni-Cd batteries. The curves are shown to demonstrate the flat voltage characteristics at end of battery capacity for Ni-Cd batteries.

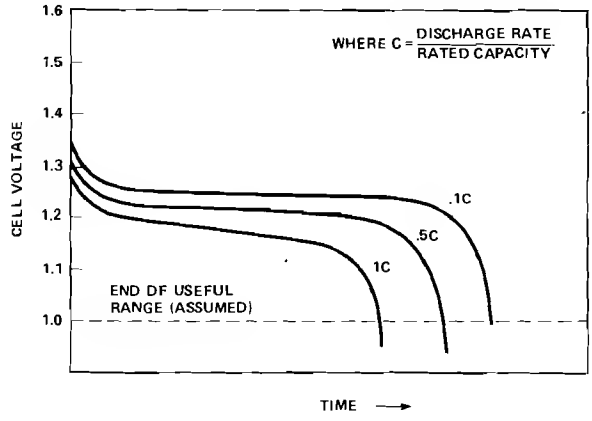


Figure 25. Ni-Cd Voltage Discharge Characteristic

Since the single cell voltage of a Ni-Cd battery is approximately 1.2 volts (as shown in Figure 25), it is necessary to boost the voltage with external circuitry (discussed previously) or stack the cells in series to obtain the proper operating voltage for the 5101L. If it is desired to stack the cells in series to obtain a higher voltage, care should be exercised to assure that the cells are reasonably matched. Cells which are not matched can cause problems during charging when placed more than three in series. Most manufacturers will provide Ni-Cd stacks of the desired size which should be adequately matched to avoid any charging problems. It is important to discuss this phenomonon with the battery manufacturer if several Ni-Cd batteries are to be used in series.

Trickle Charge Nickel-Cadmium

Ni-Cd batteries used as standby support power for memory systems should be provided with a continuous charging current from the main power source. This assures that the self discharge characteristic of the battery does not deplete battery capacity. The trickle charge current should be a constant current at a rate of one-tenth the total battery capacity (e.g. a 400mA-hr Ni-Cd should be trickle charged with 40mA current). A simple trickle charger is shown in Figure 26. If the system is to be operated at high temperature, care should be taken to assure that the maximum battery cell temperature is not exceeded during charging.

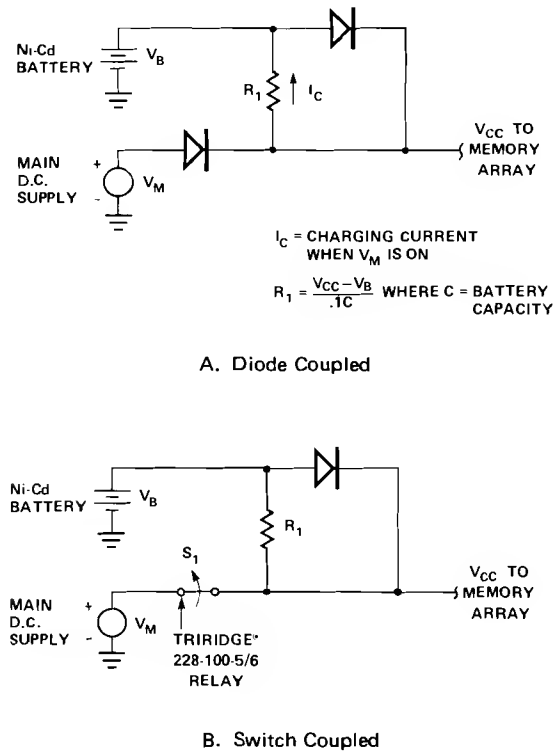


Figure 26. Ni-Cd Trickle Charger

Fast Charge Nickel-Cadmium

Some Ni-Cds can be charged at a much faster rate than that described above. However, the charging current must be monitored and reduced to trickle charge when the battery is fully charged. Failure to properly handle the charging of Ni-Cd batteries can present safety problems. The manufacturer should be consulted for recommended fast charge techniques.

Lead-Calcium

Lead-calcium batteries are also ideally suited for use as a standby power source for semiconductor memories. A popular brand of lead-calcium cell is the Gel/Cell® made by Globe Battery (Gel/Cell® is a registered trademark of Globe-Union). These types of batteries have several highly desirable characteristics such as:

1. Small size-to-capacity ratio.
2. Low standby self-discharge characteristics.
3. Flat operating discharge characteristics.
4. No permanent cell reversal.
5. Good operating temperature range.

Several manufacturers supply lead-calcium type batteries. However, for the purpose of this application note only the characteristics of the Gel/Cell® will be discussed.

Gel/Cell® Characteristics

A small Gel/Cell® battery is shown in Figure 27. The nominal cell voltage of this type of battery is 2.0 volts (the capacity of the battery shown is 1 amp-hr). This battery is ideal for use in those systems having a relatively high discharge load (~1mA). The output discharge characteristics are shown in Figure 28.

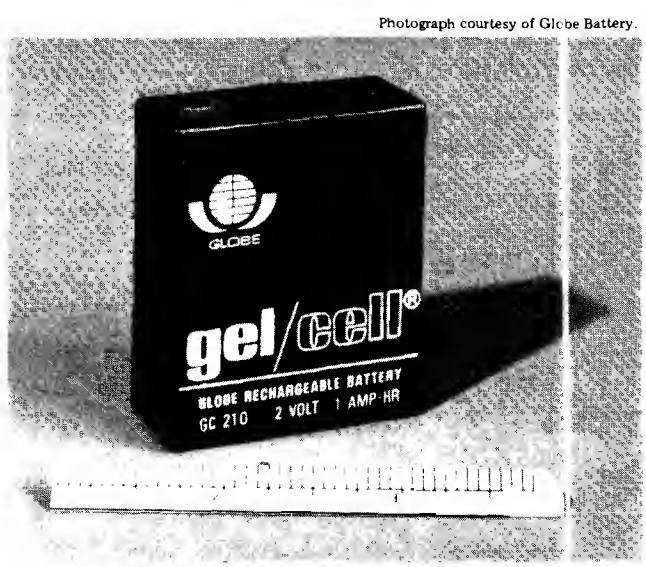


Figure 27. Gel/Cell® Lead-Calcium Battery

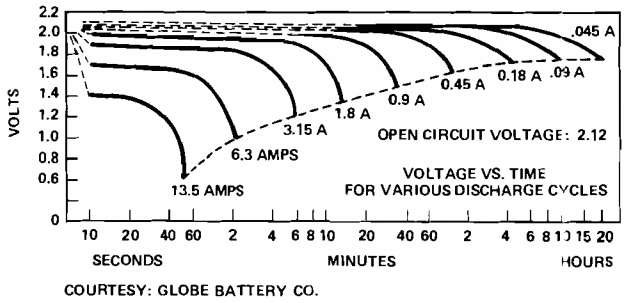


Figure 28. Gel/Cell® Voltage Discharge Characteristics

Note that the minimum discharge rate shown in Figure 28 is a hefty 45mA. At this rate the battery can supply power for 20 hours. At the rate of 1mA, this battery will last 1000 hours or approximately 6 weeks. Lower discharge rates will of course increase the battery life time proportionally.

These types of batteries are optimally used in systems having a large current drain. Although the batteries are indeed very small for a given capacity, the cell voltage is a nominal 2.0 volts which is the minimum acceptable for maintaining data in the 5101L. Therefore, either two batteries are required (series connection) or the voltage boost circuit described earlier must be used. In those systems having very small current drains in standby, the addition of a second battery will most likely take up too much room on the p.c. board. For these systems other types of batteries are recommended (such as Ni-Cd, Mercury, etc.).

Capacity of a Gel/Cell® as a function of temperature is shown in Figure 29. As is shown in this figure, at low temperatures the battery loses a great deal of capacity. Therefore, when designing systems using this type of battery, proper attention will have to be paid to the environmental temperature extremes expected in the system and proper battery selection made.

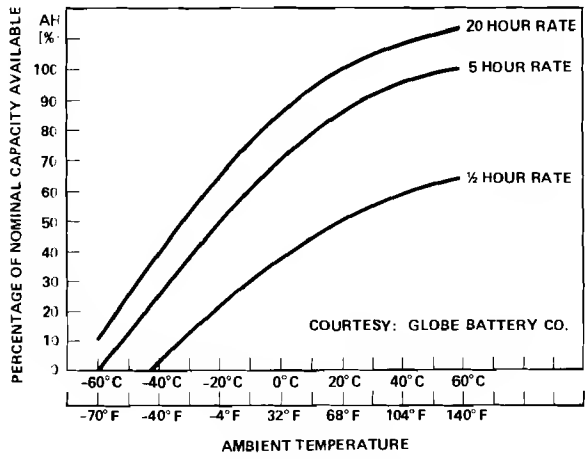


Figure 29. Gel/Cell® Capacity Vs. Temperature

Trickle Charge Lead-Calcium

Unlike Ni-Cd batteries, which accept a constant current trickle charge, the lead-calcium battery is trickle charged by a constant voltage source. The voltage required is 2.25 to 2.30 volts per cell. At this voltage, referred to as the float voltage, a Gel/Cell® will accept only the amount of charge necessary to maintain capacity.

The implementation of a trickle charger for lead-calcium batteries in a system is not as straight forward as for Ni-Cd batteries. A simple charger is shown in Figure 30. In this figure, the "float" voltage is maintained by zener Z, and potentiometer P. The potentiometer is used to adjust the voltage at node (1) to the proper level (2.25 to 2.30 volts per cell). Most zeners are accurate to no more than ±5% which is not adequate for the desired "float" voltage. Diodes D_1 and D_2 isolate the battery and power supply from each other.

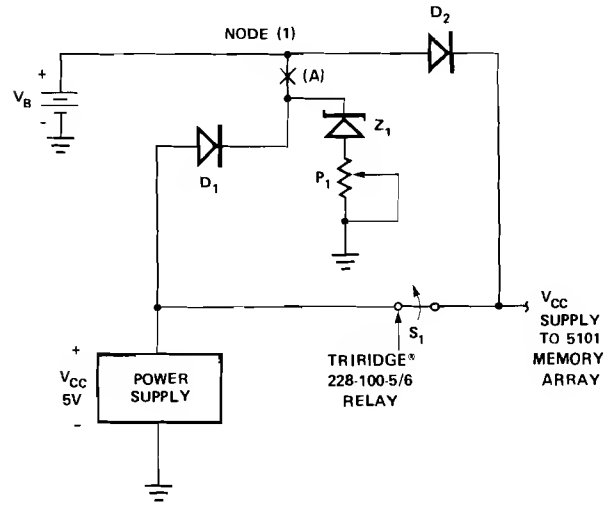


Figure 30. Lead-Calcium Trickle Charger

It is important to select a very low leakage zener (Z_1) to minimize the parasitic load on the battery during power down operations. Indeed, it may be desirable to insert a normally open switch at location (A), Figure 30, to disconnect the zener from the battery during standby operation. The switch would be controlled identically to S_1, as shown in Figure 30.

It is clear from the example given that providing a trickle charge to a lead-calcium battery and having the battery ready for instantaneous operation is more complicated than for Ni-Cd batteries. Other charging methods are available (see bibliography 4) but they all require that the battery and system voltage be identical and in 2 volt increments. Since operation of the 5101 is $4.75 \leqslant V_{CC} \leqslant 5.25$ and standby operation is $2.0 \leqslant V_{CC} \leqslant 5.25$, the charger/supply combinations described in the reference have limited value for the present applications.

Summary: Lead-Calcium

Lead-calcium batteries are particularly useful with those systems which have a relatively high standby discharge rate (greater than 1mA). The high energy density of these batteries also lend themselves to providing power in normal operation (taking into account V_{CC} requirements of the 5101L) of some systems.

The primary disadvantage of lead-calcium cells is the relative complexity of supplying a trickle charge to the batteries in those systems where the standby voltage is lower than the operating supply voltage V_{CC}.

System Implementation

The 5101 is an extremely easy to use static RAM. No refresh timing is required, only one power supply (+5V) is needed, and the device is fully TTL compatible. In addition, current transients on the V_{CC} (+5V) pin are minimal and require no special decoupling techniques. Therefore, this section will concentrate on interface techniques to the 5101 in order to minimize the power in power down/standby applications.

1K X 16 MEMORY SYSTEM

The discussion on interface techniques to the 5101 is illustrated with a 1024 word X 16 bit system shown in Figure 33. The memory array is configured as shown in Figure 33. Note that for a read/write access one of four columns is enabled by one CE_2 (CE_2A, CE_2B, CE_2C, CE_2D). The other chip enable ($\overline{CE}_1$) and the output disable pin are tied to ground to simplify the layout. All corresponding addresses are bused together and driven by one buffer as are the read/write inputs. Data in and data out pins are OR tied along a given row. Access is then simply a matter of providing the correct address (A_0-A_7), selecting a read or write function and enabling the proper row. Two simple methods for providing the proper CE_2 signals are shown in Figure 31.

TTL Interface

Interface circuits shown in Figure 33 can be implemented with either CMOS or TTL devices. If access/cycle time of the memory system is to be minimized, then series 74 or 74S type TTL can be used. However, for power down operations where a battery is used for back-up power the V_{CC} (+5V) supply to these TTL devices must be independent of the V_{CC} supply to the memory array. This is most easily accomplished by a slight modification to the power supply diagram shown in Figures 26 and 30 as modified in Figure 32. As shown, when the main supply V_m goes off, switch S_1 is opened (isolating V_m from the memory devices).

The state of the addresses, read/write, $\overline{CE}_1$, output disable and data-in to the 5101 memory array are in a "don't care" condition for standby/power down operation. Only CE_2 is required to be low ($\leq$0.2V) for the low power state. For CE_2 TTL interface drivers, a resistor to ground is required to maintain CE_2 at the proper level when power is removed from the series 74/74S gates. The resistor value required is calculated by considering two requirements:

1. CE_2 high ($V_{IH} \geq$2.2V) during operation.
2. CE_2 low ($V_{IL} \leq$0.2V) during standby/power down.

The first requirement above is determined by the maximum source current capability of the TTL drivers (I_{OH}) allowed which guarantees the proper high level output. Requirement 2 above is a function of the maximum leakage on the CE_2 line from the four 5101 devices driven by the CE_2 line. The range of values for the pull down resistor is 6.2kΩ $\leq R \leq$50kΩ for Series 74 drivers.

The POWER VALID input signal (shown in Figure 33) is derived from a power loss detect circuit. The power loss detect circuit should be able to detect a power loss before the output V_{CC} falls below 4.75V (lowest guaranteed operating power level for TTL circuits). A power loss detect circuit to implement the POWER VALID signal is discussed in the POWER LOSS DETECT section.

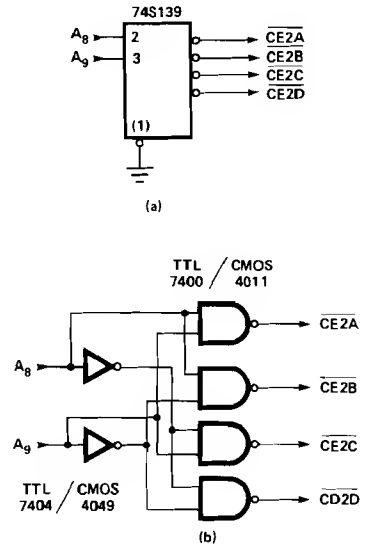


Figure 31. Chip Enable Generators 1K X 16 Memory

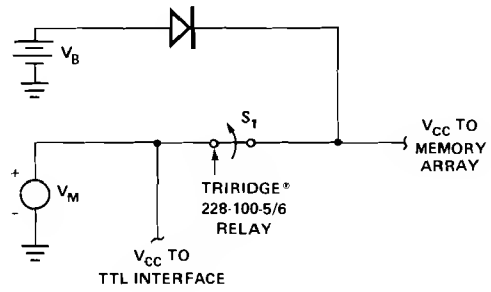


Figure 32. Power Distribution for TTL and CMOS Interface

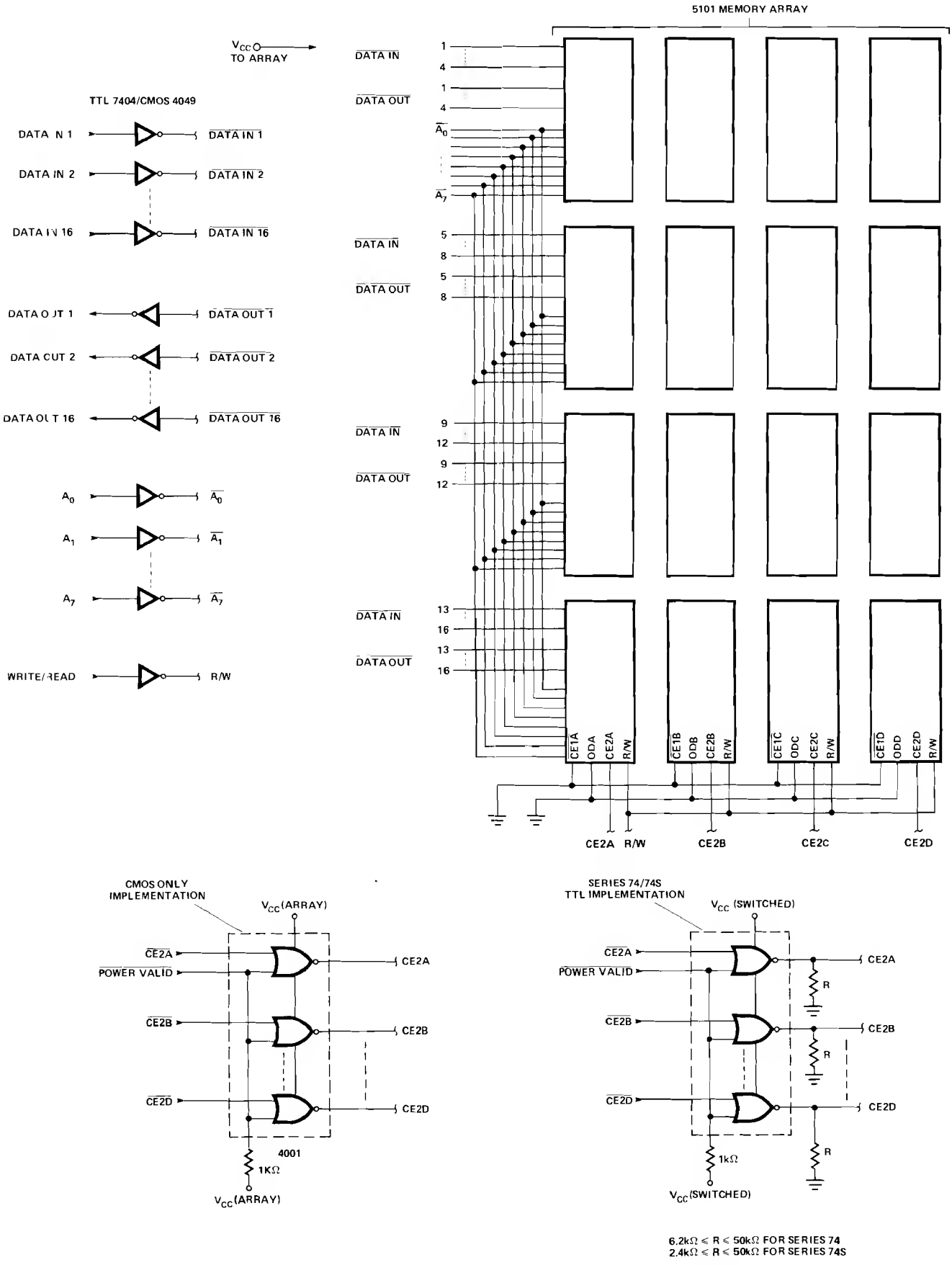


Figure 33. 1K X 16 5101 Memory System

CMOS Interface

Using CMOS circuits to interface to the 5101 memory array eliminates the need of switching out V_{CC} to the interface during power down/standby. The ultra low power CMOS interface will dissipate approximately the same power as the memory array (assuming 1K X 16) and can easily be handled by the back-up battery.

Photos of CMOS waveforms driving the 1K X 16 5101 memory array are shown in Figure 34. Also included in the photo is the noise generated on the V_{CC} supply during operation. As is shown, noise on the power line is virtually non-existent.

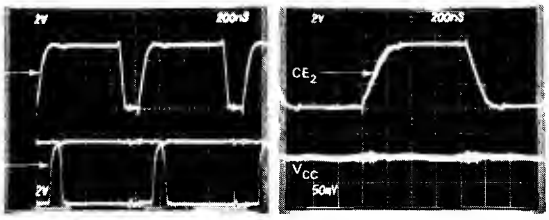


Figure 34. CMOS Interface Driver Waveforms

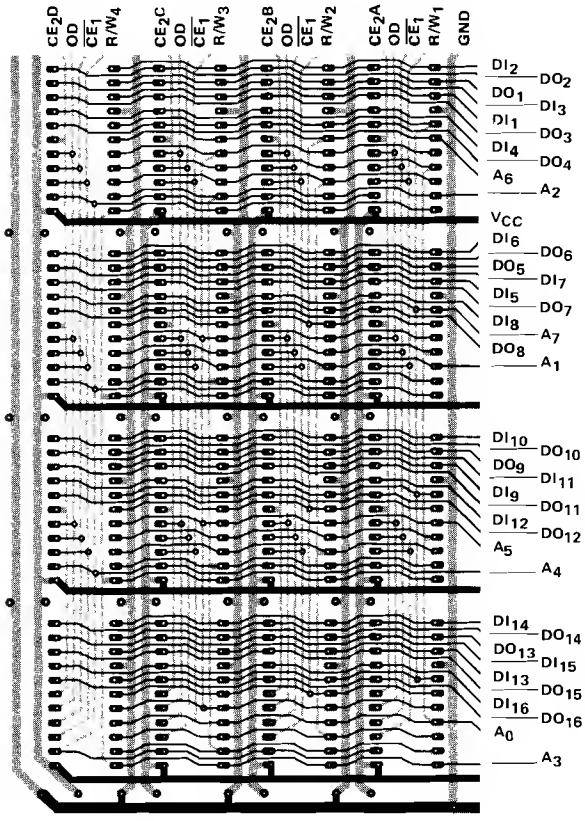


Figure 35. 5101 1K X 16 Array Layout

1K X 16 MEMORY ARRAY LAYOUT AND CARD ASSEMBLY

The layout used on the 5101 1K X 16 system described previously is shown in Figure 35. Note that V_{CC} and ground are distributed in a grided matrix and decoupled as shown. More decoupling was used in this system than is ordinarily required so the designer can use his own judgement in this regard.

The 1K X 16 memory card used was configured per the diagram in Figure 36. Notice that the card is completely self contained for standby/power down operation with the battery included on the card. With this configuration the card can be unplugged, transported to another location (with data being maintained by batteries) and operation resumed.

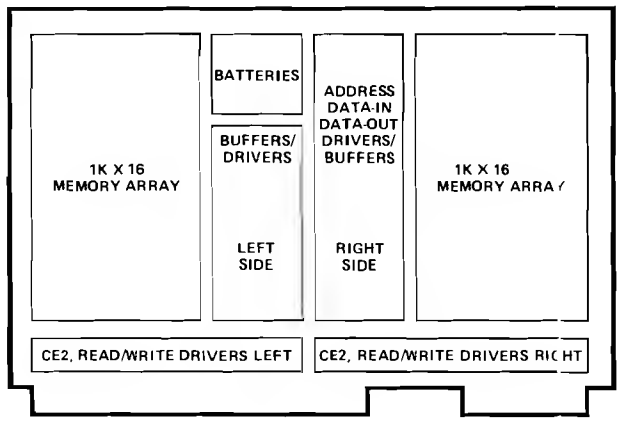


Figure 36. Dual 1K X 16 5101 Memory Card

5101 ORGANIZATION ADVANTAGES

The organization of the 5101 as 256 words X 4 bits has distinct advantages over memory devices organized as 1024 words X 1 bit in many systems applications. These applications include terminals, CRT displays, microprocessors and others which have most (or at least a portion) of their memory expandable in 256 or 512 word increments. For these cases, the number of devices required for a 256 X 4 memory device is much smaller than for a 1024 X 1 memory device.

SUMMARY

There are many selections of 5101 256 word X 4 bit devices available. Table VIII is the product selection guide for this family of devices. As shown, the designer has a wide range of choices in selecting the device most suited to his particular requirements.

Table VIII. 5101 Product Selection Guide

PART NUMBER	STANDBY CURRENT NA/BIT	+2V POWER DOWN OPTION	ACCESS TIME (NS)
5101-1	15	No	450
5101L-1	15	Yes	450
5101-2	200	No	450
5101L-2	200	Yes	450
5101	15	No	650
5101L	15	Yes	650
5101-3	200	No	650
5101L-3	200	Yes	650
5101-8	500	No	800
*M5101-4	200	No	800
*M5101L-4	200	Yes	800
*M5101-5	1000	No	800
*M5101L-5	1000	Yes	800

*Temp Range –55 to +125°C

BIBLIOGRAPHY

1. Duane L. Barney, et al, NICKEL-CADMIUM BATTERY APPLICATION ENGINEERING HANDBOOK, General Electric Co., 1971.
2. EVEREADY BATTERY APPLICATIONS ENGINEERING DATA, Union Carbide Corporation, 1971.
3. Gustav A. Mueller, THE GOULD BATTERY HANDBOOK, Gould Incorporated, 1973.
4. GLOBE GEL/CELL® RECHARGE INSTRUCTIONS, Globe Battery, Inc.

Non-Volatile Memory Using the Intel® MCS-40™ with the 5101 RAM

APPENDIX

Chon Hock Leow
Application Engineer

INTRODUCTION

The unpredictability of power failure in a volatile memory based system can result in a loss of irreplaceable information. Terminals, portable equipment and data collection instruments are but a few devices that require low cost non-volatile storage. Most read/write semiconductor memories are volatile i.e., information is lost when power is removed. Intel's 5101, 1K (256 x 4) CMOS static RAM with its extremely low standby power dissipation, typically 25μW, makes it feasible to retain information for weeks (444 days) using ordinary pen-light batteries on a "battery standby" mode. The use of a simple battery subsystem to maintain information can be a significant system cost reduction.

This note describes a technique for utilizing the 5101 RAM in a MCS-40 microcomputer based system. The MCS-40 is a four bit microcomputer system consisting of an array of CPUs, ROMs, RAMs, I/O devices and Peripherals. The specific MCS-40 configuration discussed here, offers a means of maintaining processor data via batteries in a power standby mode.

4289 AND 5101 INTERFACE

The MCS-40 utilizes a 4289 standard memory interface chip to accommodate the 5101 RAM. The RAM being CMOS and the 4289 being PMOS necessitates family interface considerations.

The Data Input lines (DI_0-DI_3) of the 5101 have a minimum input 'low' voltage (V_{IL}) of -0.3V, while the bi-directional I/O data lines (I/O_0-I/O_3) of the 4289 have a typical output 'low' voltage (V_{OL}) of -5V (with V_{SS} tied to +5V). With this incompatibility in voltages, buffers or clamped diodes (Germanium) are needed between the bi-directional I/O data lines (I/O_0-I/O_3) of the 4289 and the Data Input lines (DI_0-DI_3) of the 5101. This also applies to the PM line of the 4289 and the R/W line of the 5101.

The Data Output lines (DO_0-DO_3) of 5101 have a minimum output 'high' voltage of 2.4V, while the OPA_0-OPA_3 and OPR_0-OPR_3 need a minimum input 'high' voltage of 3.5V (with V_{SS} tied to 5V). Pull-up resistors are required on the OPR_0-OPR_3 of the 4289 to meet the required voltage. The DB_0-DB_3 lines of 3216 have a minimum output 'high' voltage of 3.5V, eliminating the need for any pull-up resistors.

With V_{DD1} of the 4289 tied to ground, the address and chip select lines are TTL compatible, eliminating the need for any buffering.

As can be seen in the schematic, Germanium diodes are used on the DI_0-DI_3 bus and R/W line (5101) and 3.3K pull-up resistors are used on the DO_0-DO_3 bus (5101).

The user has the option of not using the 3216 to channel data from 5101 onto the OPA_0-OPA_3 of 4289 by using an additional RPM instruction to flip the F/L flip-flop of the 4289.

INTERFACE CONSIDERATIONS

Only 1 standard CMOS NAND chip is needed to ensure CE2 of the 5101 is low during and after the process of power failure. When power is going down, one has to ensure that no random data is written into the 5101. This is accomplished by an output port and controlled by the program. In this case, a RAM output port, 4002, is used to control a simple RS flip-flop, implemented with 2 NAND gates, CD4011AE. This CMOS NAND device has to be backed up by the battery also.

The output lines (O_0-O_3) of 4002 have a minimum output low voltage of -7V (with V_{SS} tied to 5V). A clamped diode is advised although a gate-oxide protection circuit is already incorporated into CMOS integrated circuits. In this case, a silicon diode is used.

Further Details

(1) A pull-up resistor is needed per CS input of 4702A.
(2) A pull-up resistor is needed on the output of TTL driving the CMOS.
(3) Buffering is required between the outputs of 4702A and 5101. Intel's 3212 Input/Output Bipolar device meets this requirement adequately, with the added feature that more than four 4702As can be OR-tied without degrading the access time tremendously.

Battery Supply

The battery standby system used is a simple, low cost parallel diode switch. In order to drive this sys-

tem, the battery voltage and dc supply voltage should relate as follows:

V_D = 0.7V (diode drop)

$V_{max} + V_D \geq V_{battery}\ (V_{BB}) \geq V_{min} + V_D$

$V_{max} + V_D \geq V\ supply\ (V_S) \geq V_{min} + V_D$

Note: V_{max} and V_{min} refer to the 5101 and CD 4011AE.

In the event the supply drops below V_{min}., the battery will forward bias diode D1 (refer to schematic) to form a closed-circuit and the 5101 and CD4011AE will continue to function properly through the battery. If a rechargeable battery is used, the battery can be trickle charged through a resistor.

Theory of Operation

Hardware Aspect

On detecting power up, the 4201 generates a reset pulse required by MCS-40 components. This reset pulse is also translated to TTL level by transistor Q_1 to enable operation of the 5101. The CPU has to be enabled for interrupt in order to recognize any interrupt. On detection of a power failure, the CPU is interrupted and 4040 begins program execution at memory location 3. Either a Power Down Routine (PDR) starts at location 3 or it contains a jump vector to the PDR. With one 5101, more than three 4002 memories can be saved in it. The F/L line of 4289 is not used in both writing into and reading from 5101. After the PDR, the RS flip-flop has to be toggled by the 4002 to disable the CE2 line so as to ensure that no random data is written into the 5101 during the power transitions. This is done by bringing the CECTL low (refer to schematic). All the above operations have to be done before the power supply drops below the minimum required voltage for the system. The time depends on how much memory one needs to save and what other I/O procedures need to be accomplished. This implies that the DC power supply must maintain power for a limited time after a line drop occurs.

Software Considerations

As the operation of the system depends entirely on the program, careful consideration must be given to the construction of the program given the limited time that the CPU has before the voltage drops below the minimum requirement. The following program is written only to save the majority of the 4002 (specifically, 4 registers of the 16 main memory characters — 64 characters). The test line is used to distinguish whether a power failure has occurred. Test line is false (0) when no power failure has occurred and true otherwise.

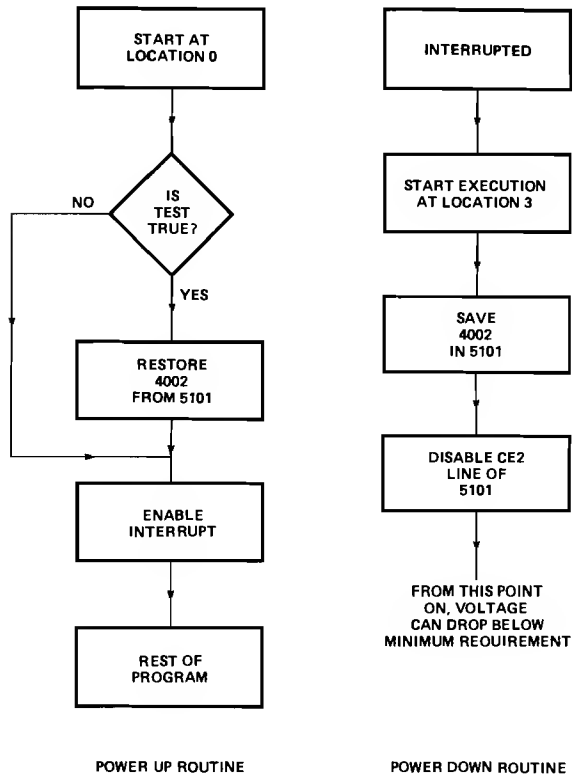


Figure 1. Program Flow Chart

The mnemonics used in the following program are those of the 4004/4040 Macro Assembler (MAC 4).

INDEX REGISTERS MAP

		14	15	
		12	13	
		10	11	
		8	9	
5101 RAM ADR	MSB	6	7	LSB
RAM PORT ADR		4	5	
		2	3	
4002 CHIP/REG ADR		0	1	4002 CHAR ADR

MAIN PROGRAM

```
        NOP                 ;No Operation
START:  JUN     CKTEST      ;Jump to check test
                            ;line
PDR:    FIM     6,0         ;A7-A0 = 00H for
                            ;CMOS RAM
        LDM     0           ;Select CM-RAM0
                            ;line
        DCL                 ;These two instruc-
                            ;tions are required if
                            ;CM-RAM line is not
                            ;0 during interrupt
        FIM     0,0         ;Save 4002s Reg. 0
                            ;in CMOS RAM
```

```
        JMS   SAVE
        INC   0          ;Save 4002s Reg. 1
        JMS   SAVE
        INC   0          ;Save 4002s Reg. 2
        JMS   SAVE
        INC   0          ;Save 4002s Reg. 3
        JMS   SAVE
        FIM   4,PORT 0   ;PORT 0=00000000B
        SRC   4          ;Set-up RAM port 0
        LDM   CECTL      ;CECTL=0001B cor-
                         ;responds to O0 line
        WMP              ;Disable CE2 line
HERE:   JUN   HERE       ;Wait for power to
                         ;go down.
CKTEST: JNT   INIT
PUR:    FIM   6,0        ;A7-A0 = 00H
                         ;CM-RAM0 is auto-
                         ;matically selected
                         ;after reset so that
                         ;no LDM 0, DCL
                         ;needed
        FIM   0,0        ;Restore 4002s Reg.
                         ;0 from
        JMS   RESTORE    ;CMOS RAM
        INC   0          ;Restore 4002s
                         ;Reg. 1
        JMS   RESTORE
        INC   0          ;Restore 4002s
                         ;Reg 2
        JMS   RESTORE
        INC   0          ;Restore 4002s
                         ;Reg. 3
        JMS   RESTORE
INIT:   EIN              ;Enable interrupt
```

From this point on, normal processing can proceed.

SUBROUTINES

```
SAVE:   SRC   0          ;Set-up 4002 RAM
                         ;character
        RDM              ;Fetch RAM charac-
                         ;ter
        SRC   6          ;Set-up 5101s
                         ;address
        WPM              ;Write into CMOS
                         ;RAM. Note that
                         ;only one WPM is re-
                         ;quired as the hard-
                         ;ware does not uti-
                         ;lize F/L flip-flop
        INC   7          ;Increment 5101s
                         ;address A3-A0
        ISZ   1,SAVE     ;Point to next 4002s
                         ;RAM character and
                         ;continue until all 16
                         ;main characters are
                         ;saved
        INC   6          ;Increment 5101s ad-
                         ;dress A7-A4
        BBL   0          ;Return
RESTORE: SRC  6          ;Set-up 5101s
                         ;address
        RPM              ;Fetch data from
                         ;5101
        SRC   0          ;Set-up 4002s RAM
                         ;character
        WRM              ;Restores it
        INC   7          ;Increment 5101s
                         ;address A3-A0
        ISZ   1,RESTORE  ;Point to next 4002s
                         ;RAM character and
                         ;continue until all 16
                         ;main characters are
                         ;restored
        INC   6          ;Increment 5101s
                         ;address A7-A4
        BBL   0          ;Return
```

Subroutine called SAVE is to save 4002s RAM characters into 5101. The data is saved sequentially starting at address 00. The above power down routine requires 478 memory cycles. With a 10.8 μs per memory cycle, the power supply has to maintain the minimum required voltage for at least 5.16 ms (478 x 10.8 μs = 5160.4 μs).

Subroutine called RESTORE is to restore 4002s RAM characters from 5101.

Note that CPU was not enabled for interrupt until after all the restoring was finished.

System Performance

The 2 CMOS chips, CD4011AE and 5101, draw a maximum of (15 + 15) μA = 30 μA, and Q1, R1, R2, R3 draw a maximum of 7.5 μA (with V_{CCB} = 4V). With a total of 37.5 μA on a standby mode, data retention can be maintained for 444 days using a 0.4 ampere-hour battery system. The 256 x 4 organization of the 5101 makes it suitable as a substitute for 4002 on standby mode.

The schematic shown can address up to 2K of ROM i.e., 8 of 4702As. R1, R2 and R3 can be optimized to draw less current depending on the transistor used.

Alternate System Configuration

The Power Down Protect Logic (PDPL) which comprises of 4002, CD4011AE and 7404 can be left out if the user does not require the power down protect capability. If PDPL were left out, the following connections have to be modified:

(1) Tie CE2 of 5101 high
(2) Connect PM of 4289 to $\overline{CE1}$ of 5101.

The 3216 can be left out if the user chooses to use an extra RPM instruction to keep track of the F/L flip-flop of 4289. If the 3216 were left out, the RESTORE subroutine would then be the following.

```
RESTORE:  SRC   6
          RPM                ;This is the dummy
                             ;instruction in
                             ;place of the 3216.
                             ;After reset, the first
                             ;RPM will read
                             ;OPA0-OPA3. Be-
                             ;cause the DO0-DO3
                             ;of 5101 are tied to
                             ;OPR0-OPR3, this
                             ;first RPM does not
                             ;pick up any useful
                             ;information. It
                             ;only serves to flip
                             ;the F/L flip-flop so
                             ;as to enable the
                             ;next RPM to ac-
                             ;cess the useful in-
                             ;formation.
          RPM                ;Fetch data from
                             ;5101
          SRC   0
          WRM
          INC   7
          ISZ   1,RESTORE
          INC   6
          BBL   0
```

Conclusion

The 5101 as an MCS-40 Data Memory element can reduce the power consumption during the power down or standby mode. The use of low cost batteries to maintain important system data during a standby mode dramatically reduces user system cost over alternative methods. This is particularly true when small quantities of memory are involved.

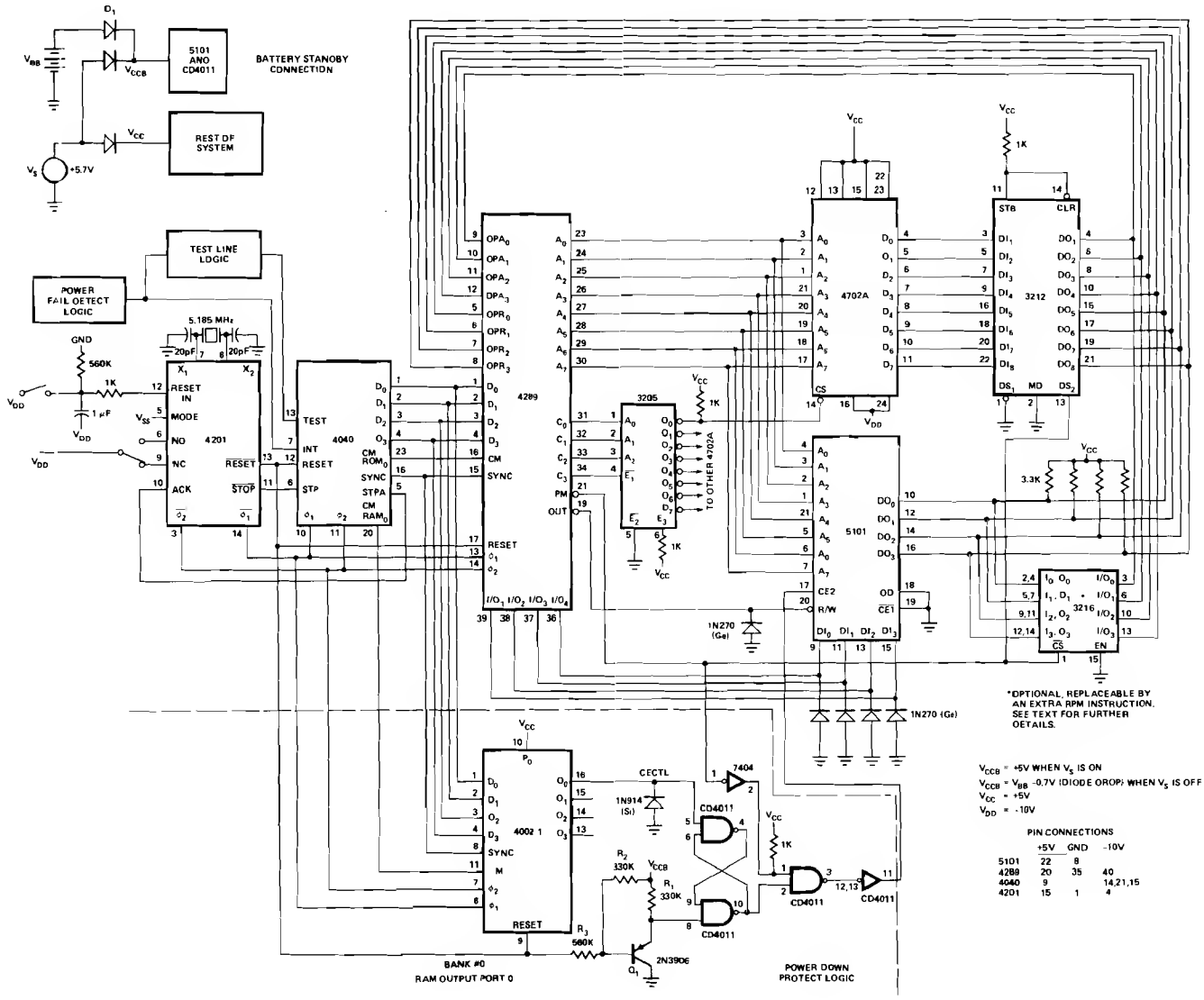


Figure 2. 4040 and 5101 Block Diagram

intel® Silicon Gate CMOS 5101, 5101-3, 5101L, 5101L-3

1024 BIT (256 x 4) STATIC CMOS RAM

*Ultra Low Standby Current: 15 nA/Bit for the 5101

- **Fast Access Time — 650 ns**
- **Single +5 V Power Supply**
- **CE_2 Controls Unconditional Standby Mode**
- **Directly TTL Compatible — All Inputs and Outputs**
- **Three-State Output**

The Intel® 5101 and 5101-3 are ultra-low power 1024 bit (256 words x 4-bits) static RAMs fabricated with an advanced ion-implanted silicon gate CMOS technology. The devices have two chip enable inputs. When CE_2 is at a low level, the minimum standby current is drawn by these devices, regardless of any other input transitions on the addresses and other control inputs. Also, when $\overline{CE_1}$ is at a high level and address and other control transitions are inhibited, the minimum standby current is drawn by these devices. When in standby the 5101 and 5101-3 draw from the single 5 volt supply only 15 microamps and 200 microamps, respectively. These devices are ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

The 5101 and 5101-3 use fully DC stable (static) circuitry; it is not necessary to pulse chip select for each address transition. The data is read out non-destructively and has the same polarity as the input data. All inputs and outputs are directly TTL compatible. The 5101 and 5101-3 have separate data input and data output terminals. An output disable function is provided so that the data inputs and outputs may be wire OR-ed for use in common data I/O systems.

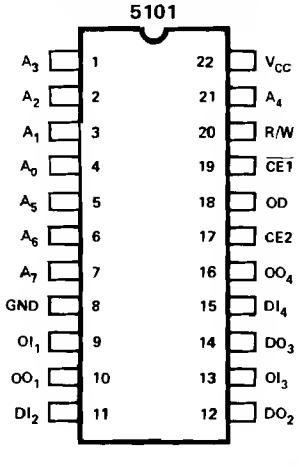
The 5101L and 5101L-3 are identical to the 5101 and 5101-3, respectively, with the additional feature of guaranteed data retention at a power supply voltage as low as 2.0 volts.

A pin compatible N-channel static RAM, the Intel 2101, is also available for low cost applications where a 256 x 4 organization is needed.

The Intel ion-implanted, silicon gate, complementary MOS (CMOS) allows the design and production of ultra-low power, high performance memories.

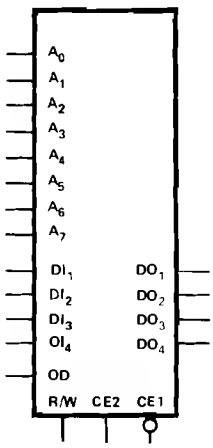
PIN CONFIGURATION

5101



LOGIC SYMBOL

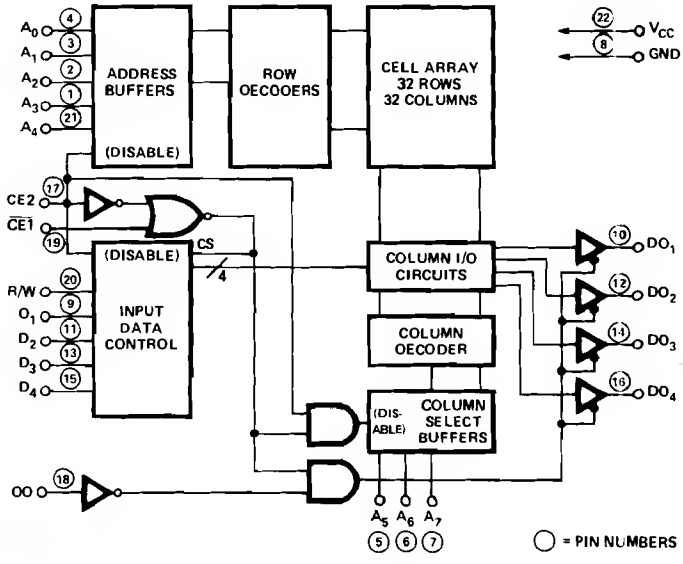
5101



PIN NAMES

DI_1 - DI_4	DATA INPUT	OD	OUTPUT DISABLE
A_0 – A_7	ADDRESS INPUTS	DD_1– DD_4	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)
$\overline{CE1}$, CE2	CHIP ENABLE		

BLOCK DIAGRAM



Absolute Maximum Ratings *

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . -0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage . . . . . +7.0V
Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics for 5101, 5101-3, 5101L, 5101L-3

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}[2]	Input Current		5		nA	V_{IN} = 0 to 5.25V
I_{LOH}[2]	Output High Leakage			1	μA	$\overline{CE1}$ = 2.2V, V_{OUT} = V_{CC}
I_{LOL}[2]	Output Low Leakage			1	μA	$\overline{CE1}$ = 2.2V, V_{OUT} = 0.0V
I_{CC1}	Operating Current		9	22	mA	V_{IN} = V_{CC} Except $\overline{CE1}$ ≤ 0.01V Outputs Open
I_{CC2}	Operating Current		13	27	mA	V_{IN} = 2.2V Except $\overline{CE1}$ ≤ 0.65V Outputs Open
5101 I_{CCL}[2]	Standby Current			15	μA	V_{IN} = 0 to V_{CC}, Except CE2 ≤ 0.2V
5101-3 I_{CCL}[2]	Standby Current			200	μA	V_{IN} = 0 to V_{CC}, Except CE2 ≤ 0.2V
V_{IL}	Input "Low" Voltage	-0.3		0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = 1.0mA

Low V_{CC} Data Retention Characteristics (For 5101L and 5101L-3) T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V		
5101L I_{CCDR}	Data Retention Current			15	μA	CE2 ≤ 0.2V	V_{DR} = 2.0V
5101L-3 I_{CCDR}	Data Retention Current			200	μA		V_{DR} = 2.0V
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[3]			ns		

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage. 2. Current through all inputs and outputs included in I_{CCL} measurement. 3. t_{RC} = Read Cycle Time.

A.C. Characteristics for 5101, 5101-3, 5101L, 5101L-3

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	650			ns	(See below)
t_A	Access Time			650	ns	
t_{CO1}	Chip Enable ($\overline{CE1}$) to Output			600	ns	
t_{CO2}	Chip Enable (CE2) to Output			700	ns	
t_{OD}	Output Disable To Output			350	ns	
t_{DF}	Data Output to High Z State	0		150	ns	
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0			ns	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns	

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	650			ns	(See below)
t_{AW}	Write Delay	150			ns	
t_{CW1}	Chip Enable ($\overline{CE1}$) To Write	550			ns	
t_{CW2}	Chip Enable (CE2) To Write	550			ns	
t_{DW}	Data Setup	400			ns	
t_{DH}	Data Hold	100			ns	
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	
t_{DS}	Output Disable Setup	150			ns	

A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

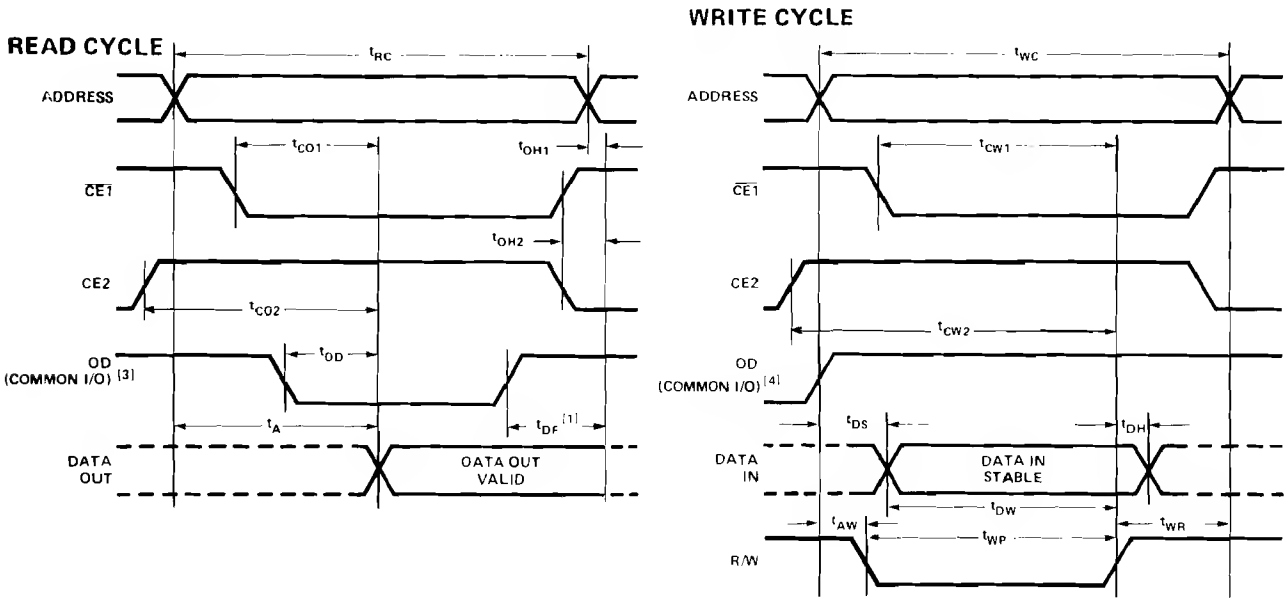
Timing Measurement Reference Level: 1.5 Volt

Output Load: 1 TTL Gate and C_L = 100pF

Capacitance[2] T_A = 25°C, f = 1 MHz

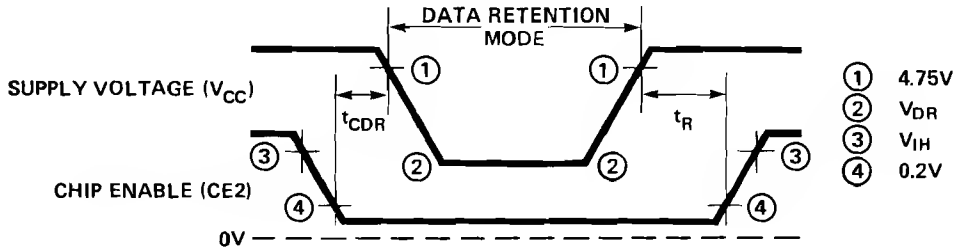
Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

Waveforms



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. OD may be tied low for separate I/O operation.
4. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

Low V_{CC} Data Retention



April 1976, INTEL CORPORATION, 3065 Bowers Avenue, Santa Clara, California 95051 (408) 246-7501

Printed in U.S.A./MMC-041-0476/5K